DESIGN AND THEORETICAL ANALYSIS OF WIDEBAND TUNABLE DUPLEXING TRANSCEIVERS

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DESIGN AND THEORETICAL ANALYSIS OF WIDEBAND TUNABLE DUPLEXING TRANSCEIVERS

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Due the proliferation of smartphones, demand for wireless data has grown dramatically. The wireless spectrum, already a scarce resource, is ever-dwindling and becoming more expensive: an FCC auction in 2015 gathered $41B for 1,611 licenses around the 1700 MHz band [1]. Projections indicate an even further increase in wireless data usage: Cisco predicts a 7-fold increase in mobile data usage from 2016 to 2021 [2]. One emerging trend to mitigate the spectrum overuse is to explore *whitespace*, locally unused frequency bands that were previously reserved for TV and maritime communications. However, the current circuit solutions to alleviate spectrum crunch such as duplexers and circulators are inherently frequency-selective, and therefore, not tunable. Also, most current wireless systems use TDD (time-division duplexing), which is not the most efficient way to use the spectrum. Frequency-division duplexing is more spectrally efficient, but in a non-MIMO system the transmitter is usually at a power level high enough to saturate or sometimes even destroy the receiver. These problems are exacerbated in full duplex systems.

In this thesis, we present a comprehensive solution to the spectrum scarcity problem by attacking on two fronts: instead of a narrow-band, fixed frequency solution, we propose a software defined radio that has a wide range of tunability. Furthermore, we take advantage of duplexing in frequency with only a single antenna to more efficiently use the available spectrum. We also analyze the

theoretical bounds of our transceiver to inform the choice of system parameters. Furthermore, we propose a novel schematic-level model to accurately simulate harmonic distortion products in switching circuits. We use this model to better predict linearity numbers in passive mixers operating in deep triode.

BIOGRAPHICAL SKETCH

The author was born in Istanbul, Turkey in 1989. She graduated from Robert College of Istanbul and moved to the United States in 2008. She studied electrical engineering and mathematics at Duke University, graduating *magna cum laude* with a B.S.Eng in 2012. Since then, she has been pursuing a Ph.D. at Cornell University in Electrical and Computer Engineering where she focuses on design and analysis of software defined duplexing transceivers. She is the recipient of the 2018 Outstanding ECE TA Award, and was the finalist for the Facebook PhD Fellowship.

To my family.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

With the proliferation of smartphones, data-hungry applications, and increasing numbers of users, spectral resources are ever dwindling. While there are many attempts from both the industry and government sides to alleviate spectrum crunch, the process is costly and slow. While spectrum is being auctioned in a piecemeal fashion, the cost for tens of MHz is billions of dollars. Since most of the current hardware is frequency static, this adaptation to a new spectrum often involves hardware overhauls, which are slow and costly. Furthermore, as the number of users grow, the number interference and collision problems increase. Ultimately, both new hardware and network-layer changes are necessary to begin solving this problem.

In this thesis, we discuss a solution to this spectrum crowding problem in the form of a duplexing transceiver. We also introduce a modeling technique that helps simulate third-order distortion products in passive mixers.

1.1 Dissertation Overview

The rest of this dissertation is organized into the following chapters:

- **Chapter 2** introduces the relevant background in the field of duplexing transceivers and explores the current state of the art.
- **Chapter 3** outlines how discontinuities in the drain current second derivative in deep-triode switching circuits lead to erroneous third order nonlinearity simulation results and introduces a circuit level model solution to

correct this behavior.

- **Chapter 4** describes the design and performance of the software defined, frequency duplex division (FDD) capable transceiver in 65nm CMOS. Two core ideas, transmission line based distributed amplifier and passive mixer based frequency selective degeneration, are introduced.
- **Chapter 5** characterizes the theoretical boundaries of the software-defined transceiver in Chapter 4 and introduces figures of merits such as isolation, cancellation, tunable bandwidth, and efficiency to compare these complex systems.
- **Chapter 6** describes the second generation full duplex design that includes a novel degeneration scheme and harmonic pre-distortion cancellation. A technique to expand cancellation bandwidth is also introduced.
- **Chapter 7** summarizes thesis contributions from previous chapters and points to future research directions in the field of duplexing transceivers.

CHAPTER 2

BACKGROUND

2.1 Motivation

With the proliferation of smartphones and other connected devices, more and more wireless data is being transmitted every day. Increasing number of users and data-hungry wireless applications, especially with the new 5G standards requiring data rates of 100Gb/s, push the current systems' capacity limits. The current trend of increasing throughput requirements is not expected to end, but to accelerate. For example, Cisco predicts a 7-fold increase in mobile data usage from 2016 to 2021 [2].

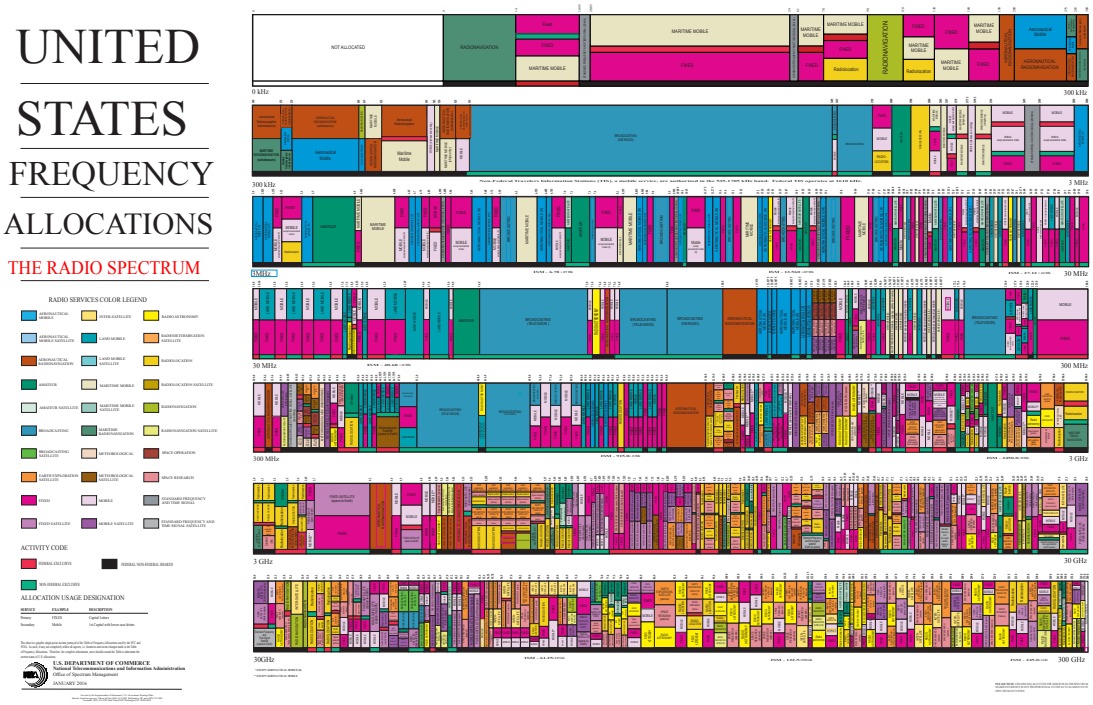


Figure 2.1: Frequency allocation map of the United States as of January 2016 [3].

The current spectrum allocations (Fig. 2.1) show how dense the current spectral map is. The spectral region around GSM bands (800-900 MHz and 1.8-1.9 GHz) and WiFi bands (2.4 GHz and 5 GHz) are especially crowded. An FCC auction in 2015 gathered $41B for 1,611 licenses around the 1700 MHz band [1]. One possible solution would seem to be to expand beyond the 3 MHz - 10 GHz frequency range. While moving to a completely new part of the spectrum (<3 MHz, >10 GHz) could seem like a valid approach, the lower frequencies have the problem of not being able to support high data rates, and the higher frequencies have very high absorption rates in the environment, thus making them unsuitable for long range wireless communications.

So, what can we do to achieve the necessary throughput requirements? There are two options:

1. Explore *whitespace*, the unused spectrum in the hundreds of MHz
2. Use what spectrum we control more efficiently through duplexing

In the next section, we will outline the challenges associated with each approach.

2.2 Exploring Whitespace

White spaces refer to frequencies that are allocated to a broadcasting service but are not in use in that region. For example, the 698-800 MHz band is reserved for TV broadcast, but currently is severely underutilized. However, there is a bigger problem - most of the currently available hardware is not frequency agile.

Observe the Samsung S9 PCB as shown in Fig. 2.2. While this phone supports many standards (4G-LTE, WiFi, Bluetooth, NFC), it comes at the cost of including several RF chips on the board. None of these chips are frequency agile: they are designed to receive or transmit at a single frequency. Exploring whitespace is not possible with fixed frequency hardware, especially since available spectrum changes temporally or geographically with fast timescales. Exploring whitespace with the existing approach requires constant hardware redesign for every iteration of upcoming spectrum availability.

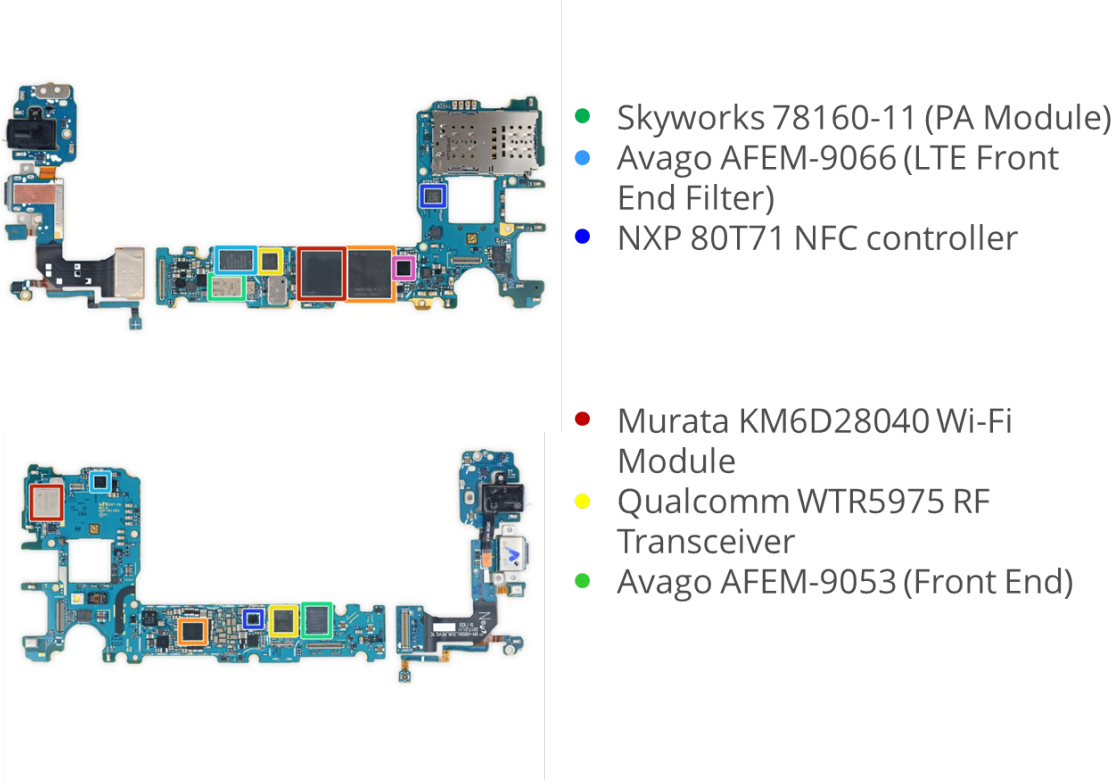


Figure 2.2: The PCB for Samsung S9. Note the variety of different LTE Modules and front ends [4].

2.3 Using Spectrum More Efficiently

Another way to increase throughput is through increasing spectral efficiency. Most ad-hoc systems such as WiFi use TDD (time division duplexing), where reception and transmission are staggered over time. In FDD (frequency division duplexing), transmission and reception happens simultaneously at different frequency bands, and in FD (full duplex) the two bands of transmission and reception are overlapped in both time and frequency.

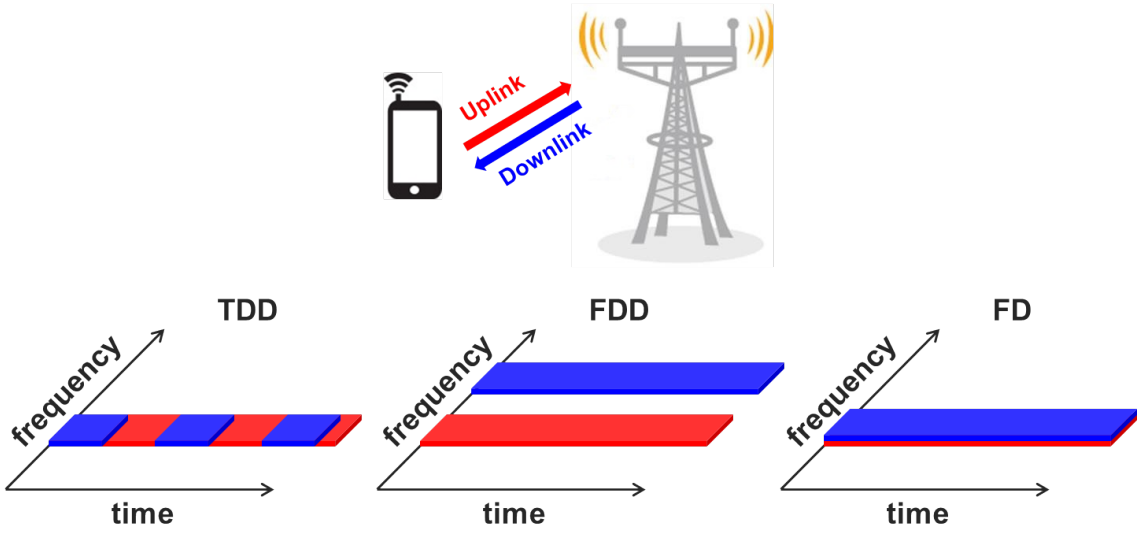


Figure 2.3: Different kinds of duplexing schemes. Left panel shows TDD (time division duplexing) where transmission and reception are staggered over time. FDD (frequency division duplexing) and FD (full duplex) use frequency duplexing to increase throughput.

Recent work [5, 6, 7, 8, 9, 10, 11, 12] proposes full-duplex communications as a means to alleviate the spectrum crunch by increasing channel capacity. In principle, full-duplex can "double the capacity of wireless networks" [13]. Achieving this ideal result, however, requires perfect self-interference. In real circuits, the degree of self-interference is the limiting factor on the capacity

gains made possible by implementing FD or FDD [14]. Indeed, the capacity gains of FD and FDD are actually limited by how good self interference cancellation (SIC) is: SINR (signal to interference to noise ratio) of >50 dB is needed to achieve reasonable (60%) throughput gains [15, 16]. Self interference cancellation is challenging: the transmit signal (>20 dBm) is at least 100 dB more powerful than the receive signal (<-90 dBm) and it must be suppressed below the receiver noise floor. To reach these high self-interference cancellation levels, SIC needs to span multiple layers of the system: RF, analog and digital (Fig. 2.4).

The next section outlines the state of the art in self-interference cancellation and duplexing structures and the associated challenges in the field.

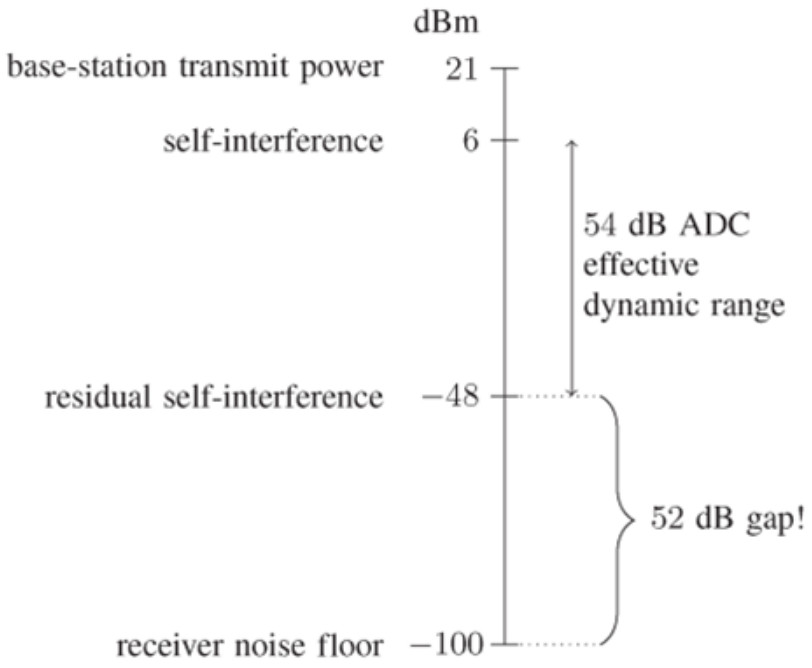


Figure 2.4: Levels of self-interference cancellation needed to reach the receiver noise floor levels [14].

2.3.1 State of the Art in Duplexing Transceivers

Single antenna interface duplexing transceivers have many challenges to overcome [17]:

1. TX saturating RX
2. TX noise appearing in the RX Band
3. TX loading RX
4. RX loading TX

The TX saturating RX (1) is the primary problem in duplexing transceivers since the TX signal is trillions of times (100-120 dB) larger than the receive signal, saturating or even destroying the receiver. The TX oscillator phase noise appearing in the RX band (2) is currently being investigated as the main reason as to why FD is a challenging problem [18, 19]. TX loading the RX (3) and RX loading the TX (4) are problems that lead to insertion loss.

Filter Bank based Front-Ends

One of the most common duplexing schemes is shown in Fig. 2.5. In this case, a bank of filters centered around a set frequency is used to isolate the transmitter and receiver. A switch chooses between the set of filters. While this approach can work for a set of frequencies, scaling is costly and insertion loss is still a problem. Furthermore, this structure is frequency static: once designed, the only way to access other bands is through adding more filters.

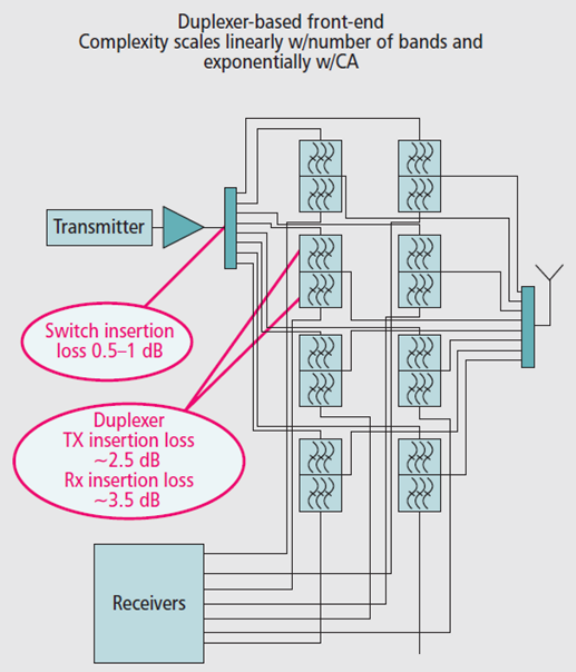


Figure 2.5: Filter bank based front-end. As the number of bands increases, so does complexity. Furthermore, an inherent insertion loss is present, reducing signal levels [20].

Electrical Balance Duplexers

One of the first approaches to duplexing with a single antenna was in the form of electrical balance duplexers [21] (Fig. 2.6). In this circuit, the TX and RX share an antenna. The RX port does not see any of the TX signal due to how the TX signal splits over the two inductors and the balance network. While these structures can achieve high output power levels, they suffer from poor tunability and a 3dB inherent insertion loss due to how the signal is split halfway between the inductor.

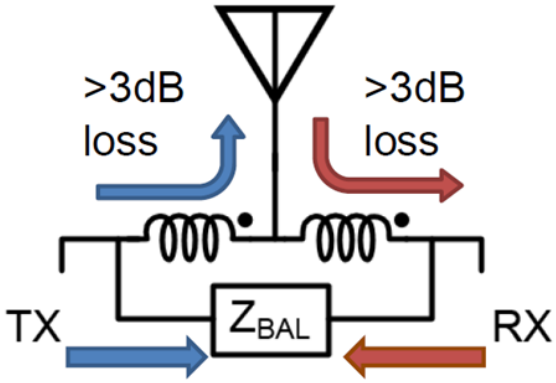


Figure 2.6: Electrical balance based duplexer. Tunability of Z_{BAL} is limited over frequency, and the 3dB insertion loss is inherent [21].

Transmission Line Based Duplexers

Recent work has showcased integratable, transmission line based circulators that are capable of high degrees of isolation with very low insertion loss. Fig. 2.7 depicts such a structure. To create non-reciprocal wave propagation, a $3\lambda/4$ transmission line is constructed around an N-path filter with a +90° phase shift, allowing propagation in only one direction [6]. However, the tuning range of this structure is limited due to the fact that the transmission line is only $3\Lambda/4$ for a specific frequency.

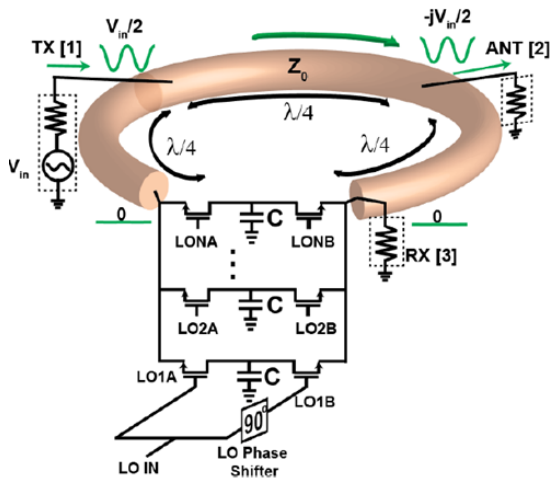


Figure 2.7: Circulator based duplexer [7].

Ultimately, most of these solutions are not frequency flexible, suffer from inherent insertion loss, or cannot support high power levels.

2.3.2 FDD vs FD: Benefits Comparison

As stated in the previous section, full duplex has been gaining a lot of interest recently due to claims of doubling channel capacity. In this recent work [22], authors compare FDD and FD and their respective benefits. Specifically, the authors list the following advantages of FD over FDD:

1. Elimination of the need to quantize the CSIT (channel state information available at the transmitter)
2. Possibility of flexible bandwidth allocation
3. Elimination of the guard frequency bands between uplink and downlink

The authors in this case assume that FDD only applies to a *fixed frequency pairs*, which is an assumption that is not always valid. In fact, points (2) and (3) are only a drawback of fixed frequency FDD. When the frequency selection for TX or RX becomes arbitrary, the only benefit of FD from this list is that the channel response is reciprocal between transmit and receive (1). This eliminates the need for quantization of the CSIT and therefore can help speed up channel estimation.

In [20], the authors talk about how FD can help realize solutions to the new challenges introduced by the 5G standard. In particular, the authors claim the following benefits for FD:

1. Increased link capacity
2. Spectrum virtualization
3. Any-division duplexing
4. Novel relay solutions
5. Enhanced interference coordination

Items (2), (3), (4), (5) are also benefits of FDD, and while (1) is realizable for FD in ideal scenarios for a single link (i.e. high self-interference and SINR), it is also a benefit of FDD for multi-node networks. Since TX-RX separation in FDD can alleviate some of the phase noise constraints while preserving many of the network benefits, further investigation of this communication paradigm (instead of the more challenging FD) is needed.

2.3.3 Network Design Improvements

Frequency duplexing is currently investigated and integrated into system-level designs by a wide range of people from information theorists to network designers. Authors in [23] propose an additional layer between the Physical (PHY) and Medium Access Control (MAC) layers to adapt to changing baseband bandwidths. This is to accommodate duplexing schemes that allow for changing bandwidth or even non-contiguous baseband signals, which is currently not possible. In the information theory field, techniques such as interference alignment [24] are becoming possible with the development of duplexing links.

CHAPTER 3

LINEARITY MODELING IN SWITCHING CIRCUITS IN DEEP TRIODE

3.1 Motivation

CMOS passive mixers have become increasingly important in a variety of applications as their properties of are better understood. Recent publications show that passive mixers are now able to attain competitive noise figures compared to the active implementations, while showing important advantages in other parameters which make them a viable alternative solution to more traditional active approaches. The most striking advantages of passive mixers stem from their bidirectionality and impedance translation properties, resulting in strikingly high out of band linearity [25, 26]. These out-of-band linearity numbers are especially useful since interference has been becoming what is limiting network throughput due to increasing number of users, and the primary method of interferers affecting each other is through nonlinearities in the system. However, circuit designers working in legacy processes are unable to simulate meaningful linearity figures for CMOS passive mixers because most models available in such processes are compact models such as BSIM3, BSIM4 from Berkeley, or MM9 from Phillips. In these compact models, the second derivative of drain current is discontinuous at $V_{ds} = 0$V, and this discontinuity manifests itself in the third harmonic is proportional to the square of the signal amplitude instead of the third power. This is especially problematic because passive mixers are biased in deep triode and therefore traverse the discontinuity, which gives rise to inaccurate 3rd order harmonic distortion behavior [27]. Indeed, this problem can manifest in any circuit which employs MOSFETs in

deep triode in a signal path, including not just passive mixers, but also circuits employing MOSFET switches for other functions.

Authors in [28] analyze that in passive mixers that are driven by square-wave LO pulses there are three main sources of nonlinearity, (1) nonzero rise and fall time of the LO (2) nonlinear device capacitances (3) nonlinear I_d as a function V_{ds}. Ultimately, (3) is the dominant factor contributing the mixer nonlinearity, which is the focus of this chapter. While there are newer, more accurate (compared to, for instance, BSIM4) surface potential based models such as PSP from Penn State, MISNAN from Carleton, HiSIM from Miura-Mattausch, they often involve implicit equations that are numerically intensive and suffer from other problems such as unrealistic transconductances [29, 30]. In addition, while they have an accurate slope for third order nonlinearities, they do not address the issue of correct magnitude for the third harmonic. Furthermore, these models are not often available to circuit designers in legacy processes, and circuit designers often do not often get a choice in the particular model they are working with. Therefore, there is a substantial case to be made for developing modeling techniques at the *schematic level* to accurately simulate 3rd order nonlinearity in passive mixers, even when using older models that have an inherently nonphysical second derivative of the drain current. There are more attempts to correctly simulate harmonic products outlined in [31], that modify and simplify surface potential models instead.

3.2 Source of the Discontinuity

The reason for this discontinuity was investigated in [32], with the conclusion that it stems from the drift velocity equation, which has an absolute value func-

tion for the electric field term:

$$v_d = \frac{\mu_0 |E|}{\left(1 + \left(\frac{|E|}{E_c}\right)^n\right)^{1/n}} \tag{3.1}$$

This equation denotes the physical phenomenon of drift velocity of the carriers saturating due to the short channel effects. Note that the second and higher order derivatives of this function are discontinuous. While the discontinuity in the numerator is compensated by an intrinsic redefinition of "source" and "drain", the absolute value in the denominator is not. Many compact models use this equation (typically with $n = 1$) to model drift velocity, causing discontinuous second derivatives.

3.2.1 Compact Model Discontinuities of the Derivatives of the Drain Current

The drain current of a transistor (for fixed gate and bulk voltages) can be represented as a Taylor series expansion (around $V_{ds} = 0$ V):

$$I_{ds}(V_{ds}) = a_0 + a_1 V_{ds} + a_2 V_{ds}^2 + a_3 V_{ds}^3 + O(|V_{ds}|)^4 \tag{3.2}$$

Fig. 3.1 shows the function Equation (3.2) approximates and compares measured data to BSIM4 simulation. While the measured data and the simulated curve match each other reasonably well for the drain current I_{ds}, comparing the second derivative of the simulated current to the measurement in Fig. 3.1 shows much greater discrepancy between the model and reality. The second derivative of the drain current I_{ds} in simulation is actually discontinuous, which implies that the term a_3 is not defined when $V_{ds} = 0$ V, whereas the second derivative

of the measured current does not have such a discontinuity. It is important to note that this continuity is also present for all derivatives greater than the 2nd. It is also important to note that the g_{ds} from simulation is an overestimate for $V_{ds} \approx 0V$.

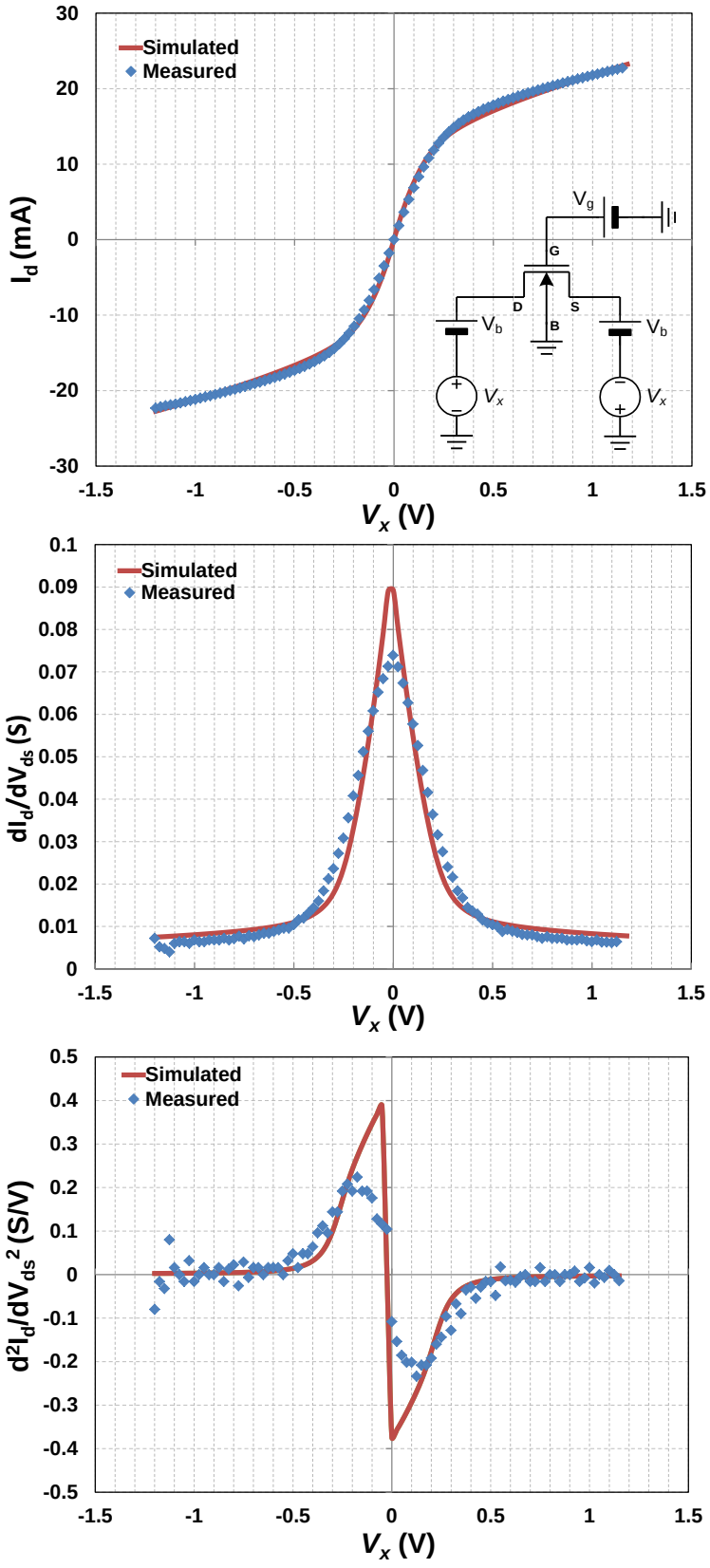


Figure 3.1: BSIM4 IV curve and derivatives for a deep sub-micron NMOS device

3.3 2nd Derivative Discontinuity Consequences on Harmonic Distortion Behavior

A surprising result is obtained when the current harmonics are simulated in a MOSFET driven by a sinusoidal V_{ds}. In Fig. 3.2, we can observe that while the fundamental tone has a 1dB/dB dependency on the input amplitude, and the second harmonic has a 2dB/dB dependence, both as expected, however, the third harmonic has a slope of 2dB/dB, instead of the expected 3dB/dB. This implies that the third-order harmonic has an A^2 dependence on the input signal, instead of the expected A^3. It is also important to note that the fourth and fifth harmonics also suffer from nonphysical behavior.

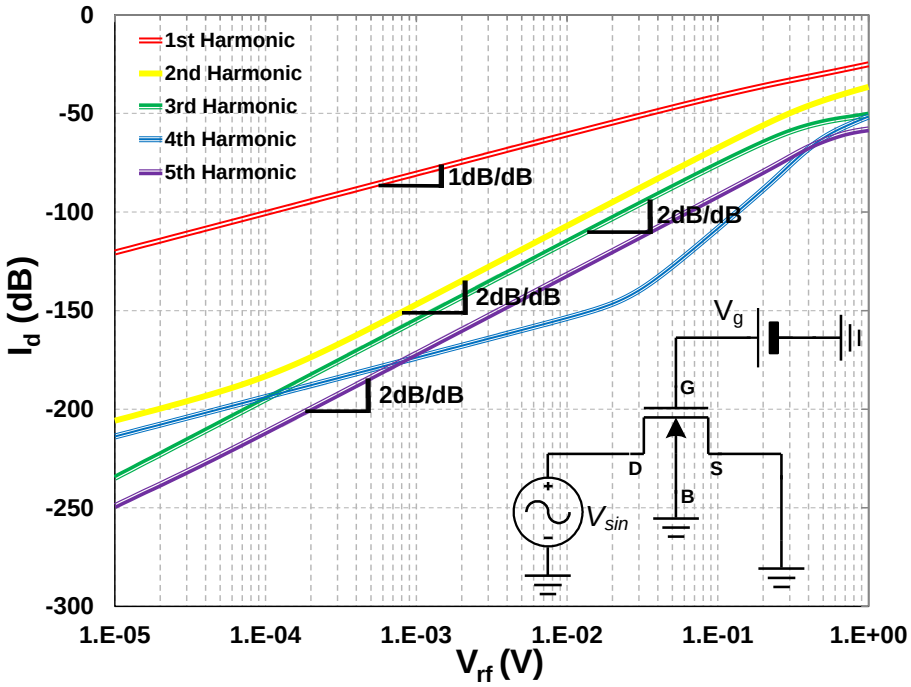


Figure 3.2: Single tone harmonic balance simulation result using BSIM4, $V_g = 1V$. A voltage input to the drain results in current harmonics. Note that the 3rd, and 5th harmonics have a slope of 2dB/dB, instead of 3dB/dB and 5dB/dB respectively.

The source of this nonphysical behavior was investigated in [32], [33] and [34], where it has been shown that 3rd harmonic does have an A^2 dependence on the input amplitude. In this section, we present a simple proof that the 2dB/dB slope of the third harmonic is indeed caused by the discontinuity in the second derivative.

We start by separating d^2I_{ds}/dV_{ds} into two constituent parts (see Fig. 3.3), continuous and discontinuous:

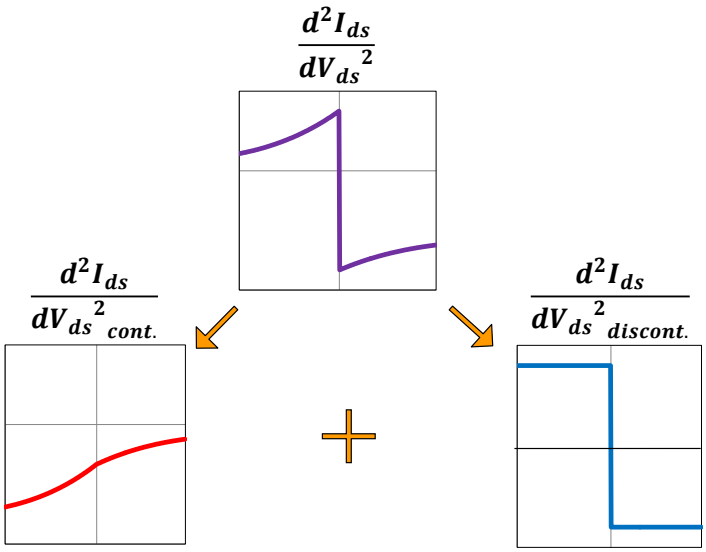


Figure 3.3: Separating d^2I_{ds}/dV_{ds} into two constituent parts, the continuous and the discontinuous.

$$\frac{d^2I_{ds}}{dV_{ds}^2} = \frac{d^2I_{ds}}{dV_{ds}^2}_{\text{discont.}} + \frac{d^2I_{ds}}{dV_{ds}^2}_{\text{cont.}} \tag{3.3}$$

$$d^2I_{ds}/dV_{ds\text{discont.}}^2 = \mathrm{K}_{\text{disc.}} \cdot \mathrm{sgn}(V_{ds}) \tag{3.4}$$

where $\mathrm{sgn}(V_{ds})$ denotes the signum function. The remainder (i.e. continuous

part) of $d^2I_{ds}/dV_{ds}{}^2$, $d^2I_{ds}/dV^2_{ds\,\text{cont.}}$ can be represented by a polynomial expansion, with terms accurate up to b_3. To obtain I_{ds}, we can integrate both the discontinuous and continuous parts twice and add them as shown:

$$I_{ds} = \underbrace{(\mathrm{K_{disc}}/2)V_{ds}^2\mathrm{sgn}(V_{ds})}_{\text{from } \mathrm{d^2I_{ds}/dV^2_{ds\,discont.}}} + \underbrace{b_1V_{ds} + b_2{V_{ds}}^2 + b_3{V_{ds}}^3}_{\text{from } \mathrm{d^2I_{ds}/dV^2_{ds\,cont.}}} \tag{3.5}$$

Note that $a_3 \neq b_3$, (a_3 being the third order approximation coefficient from Equation (3.2), indeed, the two terms have an opposite sign for V_{ds} close to zero. Now, when we substitute a sinusoidal function for V_{ds} such as $Acos(\omega t)$, I_{ds} becomes:

$$I_{ds} = (\mathrm{K_{disc}}/2)A^2cos^2(\omega t)\mathrm{sgn}(Acos(\omega t)) + b_1Acos(\omega t) + b_2A^2cos^2(2\omega t) + b_3A^3cos^3(\omega t) \tag{3.6}$$

Notice that $\mathrm{sgn}(Acos(\omega t)) = \mathrm{sgn}(cos(\omega t))$, since the signum function only takes on values -1 and +1, and $\mathrm{sgn}(cos(\omega t))$ is a square wave function (symmetric across the y-axis) with an amplitude of 1. The Fourier series of this function is a sum of odd harmonics of cosines, so we can see that I_{ds} becomes:

$$I_{ds} = \frac{\mathrm{K_{disc}}}{2}A^2cos^2(\omega t)\left[\frac{\pi}{4}(cos(\omega t) + \frac{1}{3}cos(3\omega t) + \frac{1}{5}cos(5\omega t) + \cdots)\right] + b_1Acos(\omega t) + b_2A^2cos^2(2\omega t) + b_3A^3cos^3(\omega t) \tag{3.7}$$

Now, expanding the higher order functions of cosines using expressions (3.8)

and (3.9), we get the expression in Equation (3.10):

$$cos^2(x) = 1/2 + (1/2)cos(2x) \tag{3.8}$$

$$cos^3(x) = (3/4)cos(x) + (1/4)cos(3x) \tag{3.9}$$

$$\begin{aligned} I_{ds} = \frac{\mathrm{K_{disc}}}{2}A^2(\frac{1}{2} + \frac{1}{2}cos(2\omega t))\Big[\frac{\pi}{4}(cos(\omega t) + \frac{1}{3}cos(3\omega t) + \frac{1}{5}cos(5\omega t) + \cdots)\Big] \\ + b_1 A cos(\omega t) + b_2 A^2(\frac{1}{2} + \frac{1}{2}cos(2\omega t)) + b_3 A^3(\frac{3}{4}cos(x) + \frac{1}{4}cos(3\omega t)) \end{aligned} \tag{3.10}$$

We can see here that we have an odd function for the discontinuous part with a magnitude square term dependence, which ultimately leads to the problem. Two main terms contribute to the third harmonic: $\mathrm{K_{disc}}(\pi/6)A^2cos(3wt)$ and $(b_3/4)A^3cos(3wt)$. The other terms can be found using the trigonometric identity, and they follow the same relationship for the continuous and discontinuous parts:

$$cos(\alpha)cos(\beta) = \frac{cos(\alpha+\beta) + cos(\alpha-\beta)}{2} \tag{3.11}$$

Therefore, we can see that the 3rd harmonic term has a A^2 dependency when $\mathrm{K_{disc}}(\pi/6)A^2 > (b_3/4)A^3$.

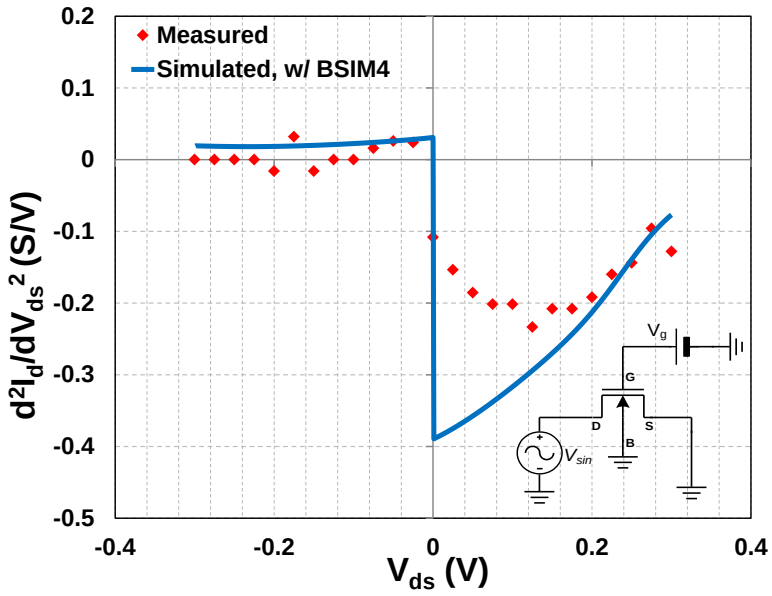


Figure 3.4: Unsymmetric drive of the drain of the MOSFET, second derivative of the drain current.

We saw in Section II the effects of the discontinuity of the second derivative of the drain current. However, the second derivative shown in Fig. 3.1 is obtained by performing the Gummel Symmetry Test, which is the test of a symmetric drive of source and drain and does not reflect how the drain and source of the passive mixer switches are typically driven [35]. Typically, for out-of-band signals, drain and source voltages are asymmetric, but the discontinuity problem still persists, as shown in Fig. 3.4. Therefore, the same problems of harmonic inaccuracies are also still present.

3.4 Model Description

3.4.1 Underlying Principle

As stated in the previous section, when the second derivative of I_{ds} with respect to V_{ds} is discontinuous, the Taylor Series terms do not exist after a_2 and consequently 3rd order harmonic distortion terms behave in a non physical way. Therefore we want a circuit that modifies this discontinuity to approximate the physical slope around $V_{ds} = 0$ V. In order to achieve this, we break up the large jump discontinuity into a series of smaller discontinuities as shown in Fig. 3.5.

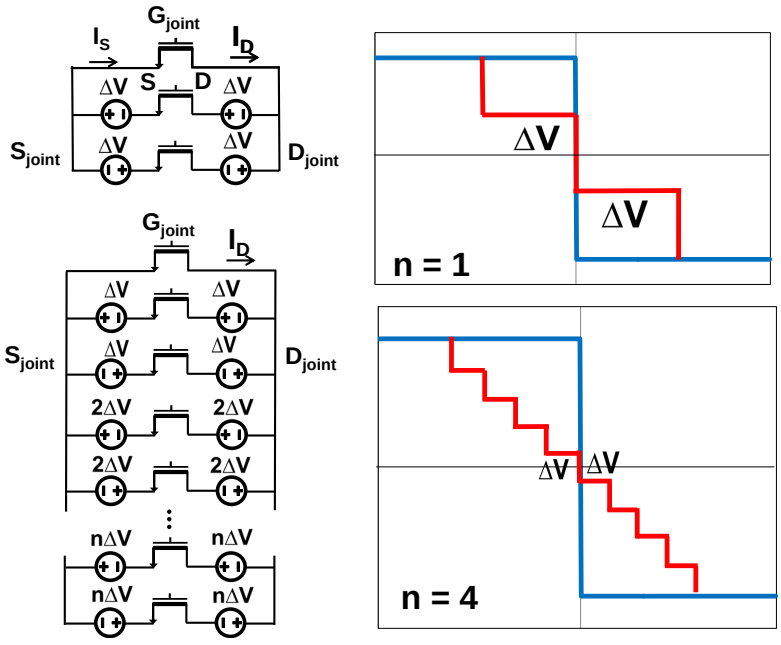


Figure 3.5: Two different cases of approximation: n=1 and n=4. Notice that in these cases the offsets are uniform. The offsets disperse the discontinuity around $V_{ds} = 0$ V while approximating the slope.

The voltage sources labeled ΔV_1 through ΔV_n in Fig. 3.6 are used to introduce symmetric offsets around $V_{ds} = 0$V, as shown in Fig. 3.5. The goal of these

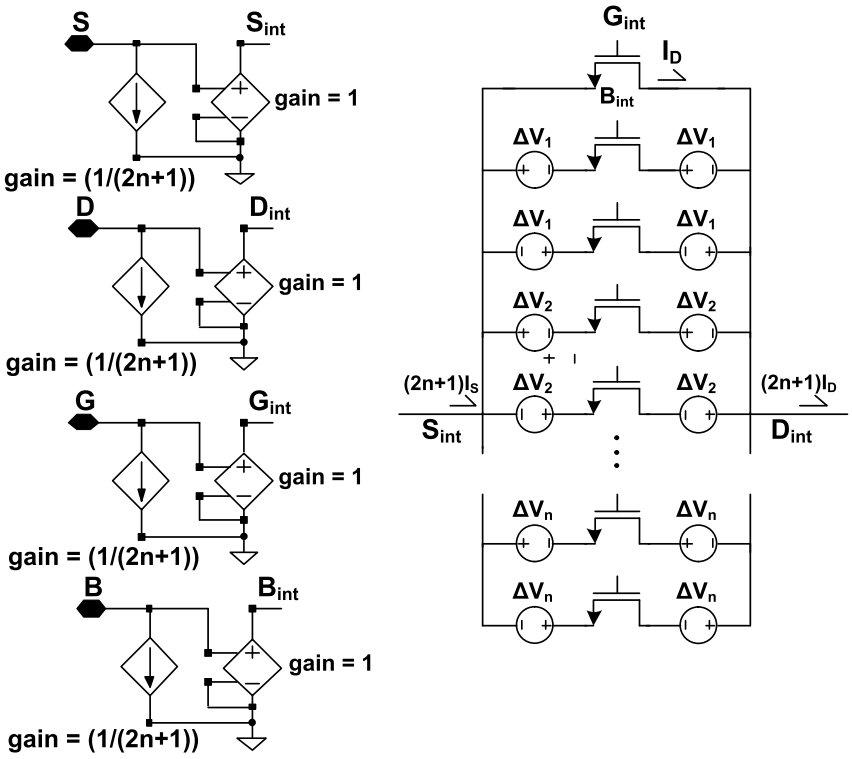


Figure 3.6: Schematic of the model to ensure continuity in the second derivative around $V_{ds} = 0\text{V}$. The combined transistors replace a single transistor in any schematic.

offsets are first to shift most of the discontinuity away from $V_{ds} = 0\text{V}$. approximate the slope of the real second derivative at $V_ds = 0\text{V}$. Approximating the slope of the measured second derivative around $V_{ds} = 0\text{V}$ is critical because the second derivative of I_{ds} is:

$$\frac{d^2 I_{ds}}{dV_{ds}^2} = 2a_2 + 6a_3 V_{ds} + \dots \tag{3.12}$$

The slope of the second derivative (i.e. a_3 term) determines the magnitude of the third order nonlinearity.

The subcircuit in Fig. 3.6 contains several critical features. The first is that it employs n distinct offset voltages (ΔV_1 through ΔV_n). Each offset voltage is ap-

plied to both source and drain of sub-transistors using ideal DC voltage sources. For symmetry, each offset is applied in both a positive and negative configuration, finally, a single sub-transistor is included without any offset at all, resulting in a total of $2n-1$ subtransistors to model a single real transistor. In order to accurately replicate various second-order geometry effects and parasitics, each subtransistor was made identical to the overall transistor being modeled. This means that for the same voltage signals, this collection of transistors will generate currents $2n+1$ times larger than the modeled transistor. Therefore, the subcircuit also includes a circuitry to scale the current on each terminal by a factor of $1/(2n+1)$, so as to accurately reproduce the expected I-V relationships.

To confirm the utility of this approach, we investigated two configurations of the model. In the first case we looked at 4 offset values each an integer multiple of 8mV ($n = 4$, offset width $= 8\mathrm{mV}$) such that, as shown in Fig. XXX: $\Delta V_1 = 8\mathrm{mV}$, $\Delta V_2 = 16\mathrm{mV}$, $\Delta V_3 = 24\mathrm{mV}$ and $\Delta V_4 = 32\mathrm{mV}$. This implies a total of 9 sub-transistors in the subcircuit, and scaling of all terminal currents by this same factor of 9. As a second case, we looked at 4 times as many offsets each 1/4 as large and ($n = 32$, $= 1\mathrm{mV}$) for the same average slope. When driven with a sinusoidal V_{ds}, the 3rd harmonics follow the qualitatively correct slope of 3dB/dB as shown in Fig. 3.9. Notice that the BSIM4 model 3rd harmonic has a slope of 2dB/dB. Notice that the slope where $\mathrm{V_{rf}} < 2\mathrm{mV}$ for the 32-offset model and $\mathrm{V_{rf}} < 17\mathrm{mV}$ for the 4-offset model is not 3dB/dB, but revert to 2dB/dB. This is because for $|V_{ds}| < \Delta V_1$, only a single discontinuity is traversed, and the required averaging across multiple offsets is lost.

It is also crucial to realize the functionality of the zero offset as shown in Fig. 3.7. Without the presence of the zero offset, as shown in the right of the Fig. 3.7, while there is no discontinuity at $V_{ds} = 0$ V, we are very far of our goal of

approximating the slope of d^2I_{ds}/dV_{ds}. So, while the 3rd harmonic will have the correct slope at that point due to the fact that there's no discontinuity at $V_{ds} = 0\text{V}$, the result will be nonphysical. We introduce the zero offset as shown in the left of Fig. 3.7 so that we know the start of the correct region of operation, namely $V_{ds} > \Delta V_1$.

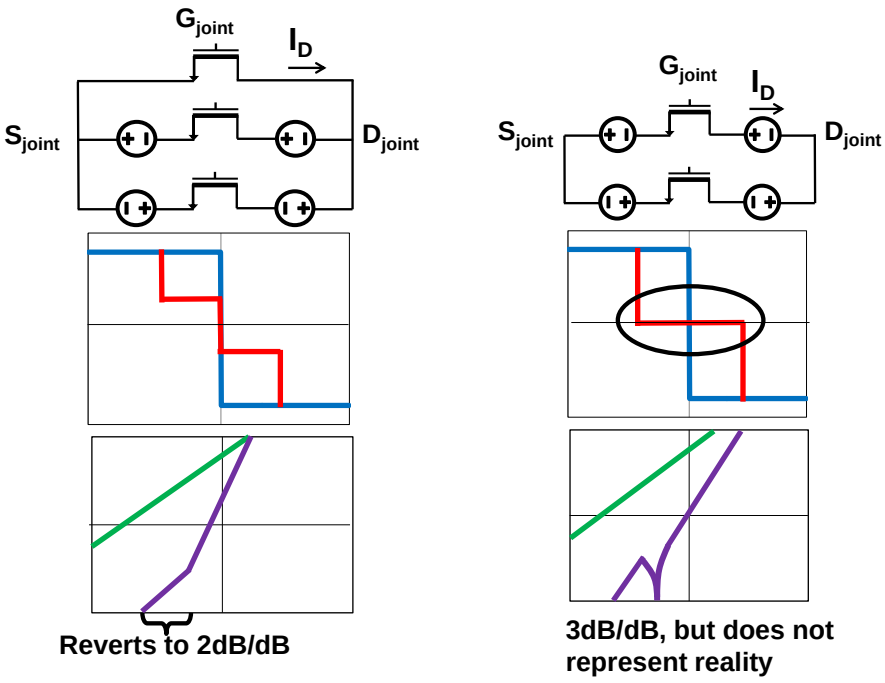


Figure 3.7: Importance of the presence of the zero offset in the model. If the zero offset is not present, there is no discontinuity at $V_{ds} = 0$ that is an indicator of the accurate region.

3.4.2 Choosing Model Parameters

In our model, we were able to choose our offset spacing and number of offsets to best reflect the *measured* second derivative slope around $V_{ds} \approx 0\text{V}$ since we had a standalone NMOS test structure. To do this, we used the simple relation

of

$$\left.\frac{dI_{ds}}{dV_{ds}}\right|_{V_{ds}=0} = \frac{\mathrm{K_{disc}}}{dV_n \cdot 2} \tag{3.13}$$

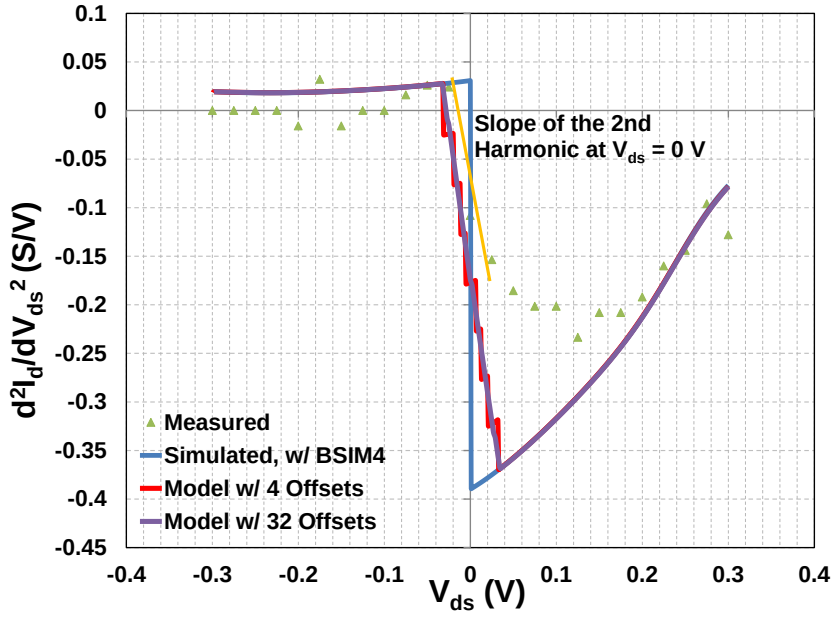


Figure 3.8: Comparison of the second derivatives. Notice that the BSIM4 second derivative is discontinuous. The yellow line denotes the measured slope around $V_{ds} = 0\mathrm{V}$.

To make sure we got a reasonable accuracy with our offsets, we chose $dV_1 < |\mathrm{V_{dsmin}}|$, the smallest $\mathrm{V_{ds}}$ we wanted to approximate over. Note that as step size decreases, the number of offsets must be increased to keep the slope constant. In this case the result will be more accurate due to the fact that a finer approximation is being performed. However this increases the computational complexity, and so simulation time, by a factor of $1 + 2n$. This fact is somewhat mitigated by the fact that replacement of the MOSFETs with our model needs to only be done to simulate RF behavior. Another important fact to note is that as long as we operate within 200 mV of $V_{ds} = 0$ V, the actual IV curve is negligibly

affected by the introduction of the offsets.

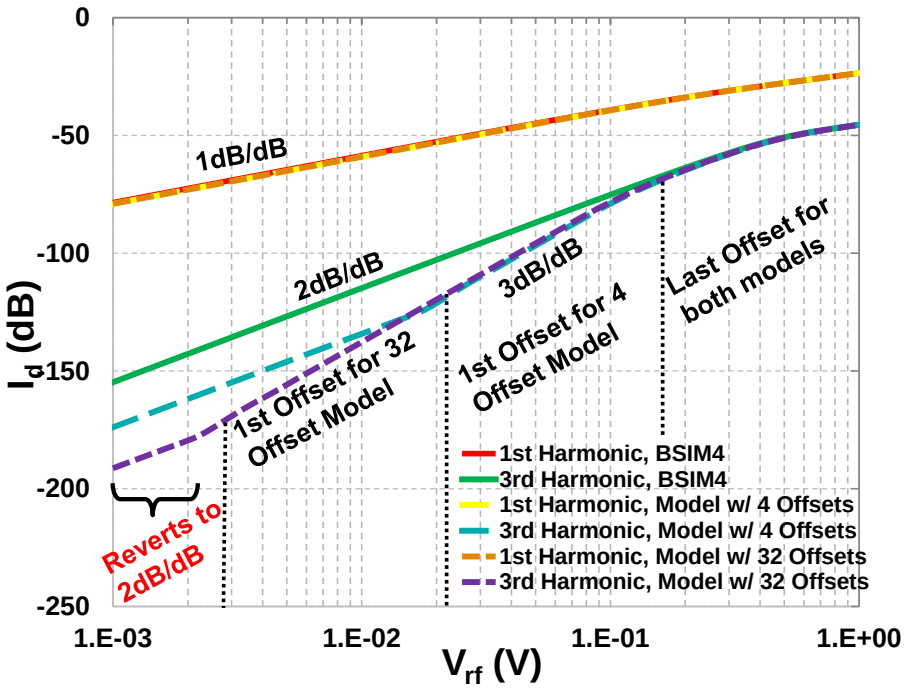


Figure 3.9: PSS simulation result using BSIM4 and the new model, $\mathrm{V_g} = 1\mathrm{V}$

3.4.3 Choosing the Correct Input Power Range

As we have explained in the beginning of the section, when we the input is a sinusoidal signal as V_{ds}, it is akin to expanding the Taylor series at a bias point of $V_{ds} = 0\mathrm{V}$. This is important to realize since the amplitude of the input signal to the drain of the transistor has to fall within a range where the model is approximating the slope of the second derivative, which corresponds to an input range of $dV_1 < |V_{ds}| < dV_n$. Since, in more complex circuits (such as mixers) V_{ds} at the RF port depends on circuit interactions as well as inputs, one should perform a transient simulation to observe the voltage at the drain node to confirm that V_{ds} falls within the accurate range for the model. Fig. 3.10 illustrates this concept

graphically.

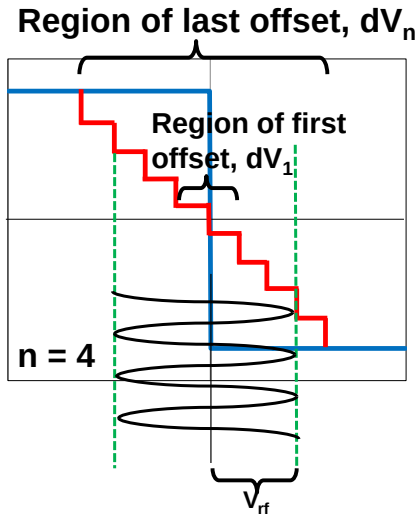


Figure 3.10: Determining the correct power input range according to V_{rf} for an n=4 example. V_{rf} has to fall between the first and the last offset for the accurate behavior.

3.4.4 Uniform and Nonuniform Offset Spacing to Estimate Higher Order Harmonics

The version of the model presented in [36] had used uniform offsets to approximate the second derivative slope. However, as shown in Fig. 3.11. we can choose offsets to be nonuniform. This has the benefit of approximating through a wider range of input powers, but also introduces the ability to approximate higher order harmonics if needed. Thus, if the 5th harmonic would need to be approximated, then, we would try to choose the offsets such that the 5th derivative of the drain current would be approximated. However, we were not able

to compare measurement results for this part because the fifth harmonic power was very close to the noise floor for acceptable power input ranges.

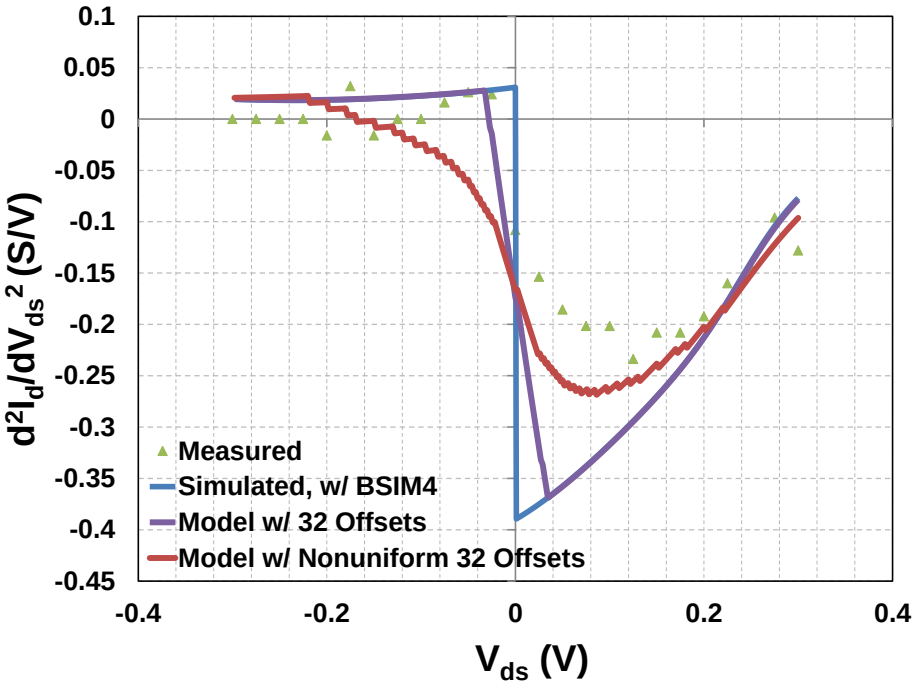


Figure 3.11: Choice of non uniform offsets to approximate higher order derivatives

3.4.5 Choosing the Parameters without Experimental MOSFET Data Predictive Modeling

In order to extend the applicability of our technique to the cases where one does not possess measured data, we also sought techniques for extracting a_3 (from Eq. 3.12)) from pure simulation. We found that the second derivative of a high (7+) order polynomial fit of the drain current from the BSIM4 simulation reasonably approximated the slope of the second derivative at $V_{ds} = 0\text{V}$. Another alternative for a predictive model is to use a different, non-discontinuous func-

tion for the velocity saturation term. Generally, the drain current expression has a velocity saturation modifier:

$$I_{DS,vsat} = \frac{I_{DS,w/o\ vsat}}{(1 + |v_{ds}/v_{sat}|)} \tag{3.14}$$

which we can replace with

$$I_{DS,vsat} = \frac{I_{DS,w/o\ vsat}}{0.5(1 + \sqrt{1 + 2(v_{ds}/v_{sat})^2})} \tag{3.15}$$

These correspond to Eq. 3.1 for cases $n = 1$ and $n = 2$. Whereas the expression in (3.14) contains discontinuities in its derivatives, (3.15) does not. So, if we can replace (3.14) with (3.15) in addition to a magnitude correction factor to fit the IV curves together, we will be able to approximate the IV curve and therefore, compute an expected slope. Since the only voltage constant in (3.15) is v_{sat}, the total number of steps multiplied by the step size should be proportional to v_{sat}. Empirically, for a v_{sat} of 180mV, we found this constant of proportionality to be about 0.5. This will vary by different numbers of v_{sat} and can easily be extracted case-by-case. Analytically, to obtain the expression for ΔV_n, we can take the third derivative of Eq. 3.15 to obtain a_3 (which is equal to $-3/v_{sat}^2$), and then observe the "height" of the jump discontinuity K_{disc} by taking the second derivative of Eq. 3.14. Using Eq. 3.13, we get

$$\Delta V_n = \frac{2}{3} v_{sat} \tag{3.16}$$

3.5 Experimental Comparison

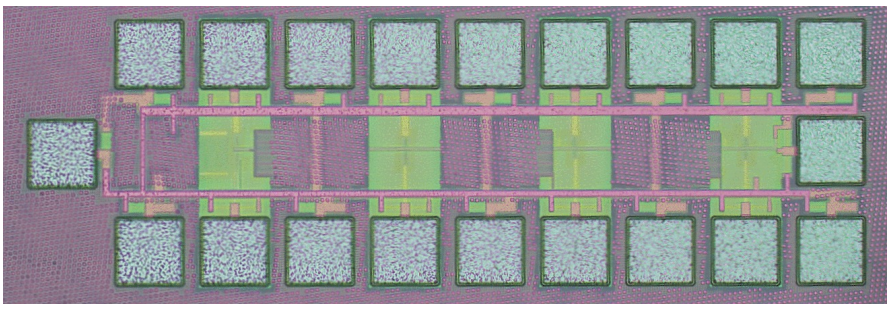


Figure 3.12: Die photo of the standalone NMOS test structure, 4 different transistor widths.

3.5.1 Single Transistor

To confirm model performance, we characterized single transistor test structures for 4 different devices. Fig. 3.8 compares second derivative curves (now for constant V_s, and varying drain voltage) for measured data, the BSIM4 model, and our approach with two different number of offsets ($n = 4$ and $n = 32$). We then measured 3rd order distortion products experimentally using low noise probes and compared them to predictions from simulations of BSIM4 and our technique using the 32-step model, as shown in Fig. 3.9. Our approach not only provides the correct 3dB/dB slope, but predicts an intercept within 2dB of the measured result.

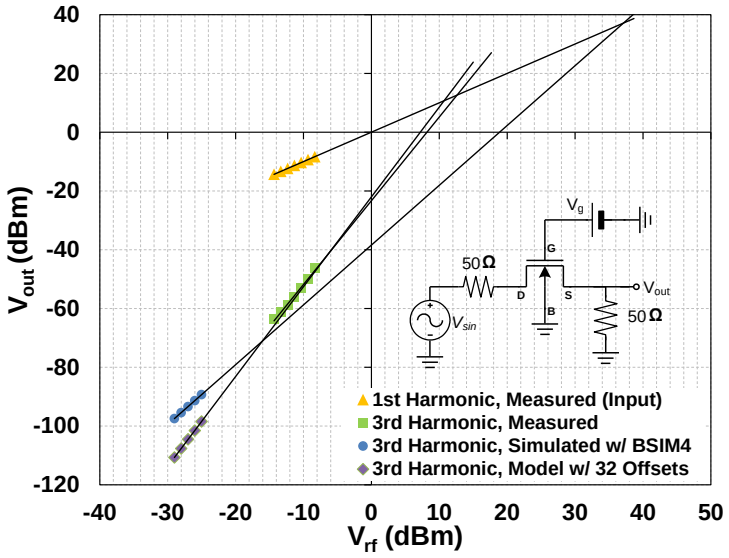


Figure 3.13: Harmonic distortion products in the single transistor, at f = 900MHz. The 3rd harmonic produced by the BSIM4 simulation has a slope of 2dB/dB, whereas the model 3rd harmonic has a slope of 3dB/dB.

3.5.2 8-Phase Passive Mixer

The CMOS mixer simulations were done once before in [32], however, this is the first time where a complete system with feedback resistors were tested.

Finally, to confirm the utility of this model for a real circuit, we implemented an 8-phase passive mixer first receiver (similar to that reported in [25]), schematic as shown in the inset of Fig. 3.14 and compared our measured results with both our model simulations and BSIM4 simulations. While the BSIM4 model predicted a 2dB/dB slope with an incorrect amplitude, with our 32-offset model, we were able to simulate the IIP3 within 4dB of the measured result (see Fig. 3.14).

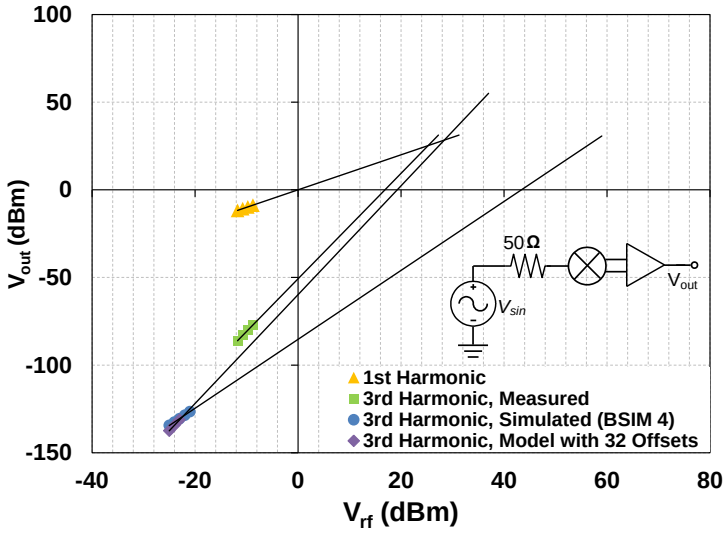


Figure 3.14: IM3 distortion products in the 8-phase passive mixer

3.6 Conclusion

We have shown how the discontinuous second derivative of the drain currents in compact models affects the behavior of the slope of the output harmonics. We then presented a simple schematic level technique which can easily be implemented by circuit designers and which approximates a continuous second derivative of the drain current at $V_{ds} = 0\text{V}$. We characterized how the magnitude of voltage offsets and number of offsets change the harmonic distortion simulation behavior. Finally, we have compared our simulated model results with measured results from a single transistor and an 8-phase passive mixer and shown qualitatively and quantitatively correct behavior of harmonic distortion. Ultimately, we were able to predict IIP3 in a passive mixer within a 4dB accuracy.

CHAPTER 4

A FULLY INTEGRATED SOFTWARE-DEFINED FDD TRANSCEIVER

Although there is much active research on software defined radios (SDR) with receive (RX) or transmit (TX) functionality, little work has been done on SDR transceivers supporting FDD. In this chapter, we present a new circuit concept in which a distributed TX circuit cancels the transmitted signal at a reverse (RX) port through destructive interference while adding signal constructively at a forward (TX) port. We pair the distributed transmitter with a receiver-tracking PA degeneration technique to suppress the injected noise from TX circuits in the RX band. The system does not require off-chip filters or circulators, but still achieves both SDR flexibility and both FDD and TDD function. Measurements from the transceiver implemented in 65nm CMOS show a frequency tuning range of 0.3-1.6 GHz with TX-RX isolation >23 dB and transmitted power up to 19 dBm.

4.1 Motivation

Most modern wireless systems must support duplex communications (i.e. Frequency Division Duplex (FDD) and Time Division Duplex (TDD)), and be able to access an ever increasing range of frequencies and standards. This latter requirement has generated interest in dynamic and scalable spectrum access, which has driven research on flexible, software-defined receivers [37, 38, 39, 40, 41] and transmitters [42]. Although there has been progress in developing RFICs to enable radios with either integrated duplex operation [43, 44, 45, 46, 47, 48, 49] or high flexibility, a fully integrated radio combin-

ing both features with high TX output power has yet to be demonstrated.

Limited spectrum availability in two-way commercial radio (i.e. GSM 900/1800 MHz, 4G-LTE) has created such demand that auctions for the 700 MHz band generated $19B in 2008 [50]. To address this, the FCC has adopted reverse-auctioning, buying back TV bands, and opening up spectrum in a fragmented fashion [50]. Transceivers that use frequency inflexible elements such as high-Q filters (i.e. SAW and BAW filters), diplexers, circulators, and/or TR switches, have a limited ability to use these new bands.

Meanwhile, FDD is used in most licensed bands for cellular communication worldwide, and offers reduced latency relative to TDD. FDD enables full data capacity for both transmit and receive, meaning that FDD deployments provide greater coverage and can achieve cell edge rates further from the base station (5dB better [51]), requiring fewer base stations, reducing cost. Current FDD implementations tend to employ symmetric up- and down-link channels, and so suffer when data rates flowing on the downlink exceed the uplink, degrading spectral efficiency compared to TDD. However, this assumes fixed equal bandwidths for both links, an assumption that is likely to change with the deployment of a true SDR FDD. Nonetheless, the benefits of FDD have been significant enough to outweigh the challenges that FDD imposes on the radios themselves.

To support FDD, a transceiver must separate receive (RX) and transmit (TX) signals. A typical FDD duplexer can be treated as a 3-port network, with a TX port, RX port, and antenna port. Strong TX signals must be delivered to the antenna without compressing, saturating or damaging the receiver. At the same time, TX and RX should not load each other, as this will degrade TX efficiency and increase RX loss as RX signals pass from antenna to RX port. Similarly, TX noise in the RX band should be suppressed at the RX input to avoid desensitiz-

ing the receiver. Finally, this isolation should be maintained in the presence of changing antenna impedance.

Commercial duplexers rely on linear passive structures, typically filters (i.e. SAW, BAW) or circulators/magnetic structures, between receive and transmit circuits to provide TX-RX isolation. These techniques are narrow band, inflexible in frequency, and difficult to integrate with circuitry, requiring banks of LNAs, PAs and off-chip elements for multi-band function [37]. Integrating these functions using electrical balance structures, incurs intrinsic losses (on the order of 5dB) with a relatively narrow, inflexible band [42, 52, 53, 54]. Recently developed circulator and duplexer circuits avoid fundamental losses, but are limited in bandwidth and TX power [55, 56]. Finally, employing multiple antennas to achieve isolation [43, 44, 46, 53] increases system size, and/or uses multiple antennas that could be better used for MIMO operation. Furthermore, most SDR/full-duplex radio efforts involve multiple antennas with antenna duplexing chips, and there exist only a few works that integrate the antenna interface on chip ([52, 53, 54, 55]).

In this Chapter, we present a circuit that combines two new techniques into a programmable transceiver capable of flexible FDD (as well as TDD) operation across a wide range of frequencies on a single antenna. The transmitter is composed of a distributed array of smaller sub-transmitters with programmable gain and phase, each of which is coupled into an artificial transmission line (TL). Careful choice of gain and phase of each sub-transmitter output allows signal power to combine in the forward direction and cancel at the reverse port, as demonstrated in [57, 58]. Noise injected by the PAs into the line is suppressed using an RX tracking degeneration scheme that selectively reduces PA transconductance in the RX band. This, combined with a passive mixer first receiver,

allows simultaneous transmit and receive across a wide frequency range for software defined FDD [48] [49].

4.2 Key Techniques and System Architecture

The presented software defined FDD transceiver employs two critical circuit techniques as well as an overall system architecture to support them, all of which are discussed in this section.

4.2.1 Distributed Duplexing Structure

To protect the receiver from large TX signals without unduly loading the TX, we propose the distributed structure shown in Fig. 4.1. The antenna and RX ports are separated by an artificial TL made up of inductors and capacitors, which provides an electrical delay and allows RX signals to pass from the antenna port to the RX port with low insertion loss. A distributed transmitter consisting of $N_{st} = 6$ sub-transmitters injects currents into different taps along the TL. The sub-transmitters are driven by the same upconversion LO and baseband input signal, while the amplitude and phase of each sub-transmitter output is independently controlled by its baseband circuitry, acting as a complex valued weight between the TX input and each injection point. As with a traditional distributed amplifier, the TX signals can be made to add in phase along the TL to deliver a strong signal to the antenna port. However, full control of the complex weight of each sub-transmitter allows the TX signal to be simultaneously nulled at the RX port.

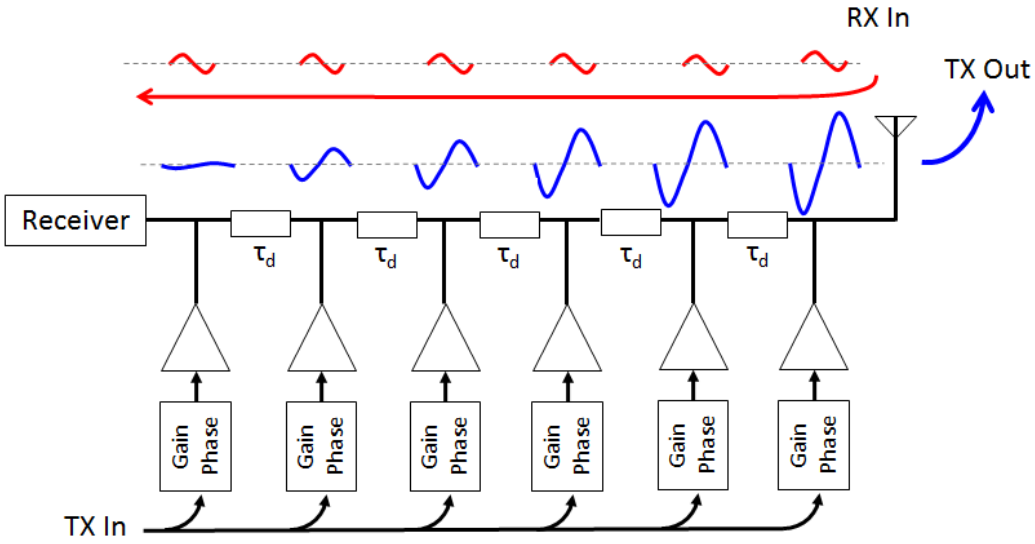


Figure 4.1: Concept for distributed duplexing transceiver. $N_{st} = 6$ sub-PAs apply weighting (gain and phase shift) to TX input and inject into an artificial transmission line made of segments with delay τ_d. TX signals add constructively at the antenna and null at the receiver. Received signals from the antenna propagate to the receiver.

1. Mathematical Foundation for TX-RX Isolation Using a Distributed TX Circuit

In order to choose appropriate weights to achieve these goals, we first model the TL as an N_{st}-terminal impedance matrix Z_{TL}. The matrix $Z_{TL}(\omega)$ incorporates the complex impedances of the component inductors and capacitors, series and shunt resistive losses, and the termination impedances of the receiver and antenna, as shown in Fig. 4.2.

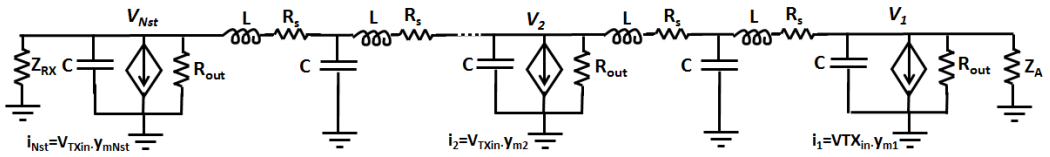


Figure 4.2: Linear circuit model of distributed duplex transceiver. TL segments composed of LC T-sections (with parasitic resistance R_S). PAs are modeled as current sources injecting weighted versions of the input. The shunt resistive losses are integrated into R_{out}.

The sub-transmitters inject N_{st} currents, $\vec{i} = (i_1, i_2, ..., i_{N_{st}})$, each proportional to the global TX input, $V_{in,TX}$, times a local complex weight, such that $i_i = V_{in,TX} y_{mi}$, where y_{mi} is the trans-admittance of the i^{th} sub-transmitter, incorporating its complex weight. These currents interact with the TL (characterized by the Z_{TL} matrix as given below) to generate the necessary N_{st} voltages. We are only concerned with two of these voltages: the voltage at the antenna port, $V_{ant} = V_1$, and the voltage at the RX port, $V_{RX} = V_{N_{st}}$. The requirements for FDD can be formulated in matrix form:

$$\begin{pmatrix} V_{ANT} \\ V_{RX} \end{pmatrix} = \vec{v} = Z(\omega_{TX}) \vec{y_m} V_{in,TX} \tag{4.1}$$

where $Z(\omega_{TX})$ relates the N_{st} injected currents to the two endpoint voltages at the TX frequency. For a 50Ω TL with matched termination impedances, $Z(\omega)$ can be approximated as:

$$Z(\omega) = 25\Omega \begin{bmatrix} 1 & \alpha \cdot e^{j\omega\tau_d} & \dots & (\alpha \cdot e^{j\omega\tau_d})^{N_{st}-1} \\ (\alpha \cdot e^{j\omega\tau_d})^{N_{st}-1} & (\alpha \cdot e^{j\omega\tau_d})^{N_{st}-2} & \dots & 1 \end{bmatrix} \tag{4.2}$$

where τ_d is the per stage delay α is the per stage loss ($\alpha < 1$) due to finite

inductor Q and PA output impedance $Z_{out,PA}$. However, the analyses presented here hold even when $Z(\omega)$ deviates from Eq. 4.2 due to impedance mismatch or lumped-element effects. The goal is to find N_{st}-entry vector, $\vec{y_m}$ that generates the desired voltage at the antenna $V_{ANT} = A_{v,PA}V_{in}$ while nulling it at the receiver $V_{RX} = 0$, accomplishing duplexing.

For $N_{st} > 2$, many solutions exist to meet these two restrictions, but a potentially desirable solution also minimizes the magnitude of the injected currents, and so of the weights, allowing minimization of bias currents and therefore increased array efficiency. Applying the pseudo-inverse gives:

$$\vec{y_m} = Z^*(ZZ^*)^{-1} \begin{pmatrix} A_{v,PA} \\ 0 \end{pmatrix} = Z^\dagger A_{v,PA} \tag{4.3}$$

where Z^* is the Hermitian of Z. This is a unique solution that minimizes the summed-squared current (i.e. the L2-norm of $\vec{i}$) while generating the required terminal voltages.

The finite bit resolution N of the complex weights $\vec{y_m}$, can limit cancellation, as imperfect weights result in an imperfect null at the RX port (which is discussed further in Chapter 5). Ideally, the cancellation is upper-bounded to $2dB + 6dB(N) + 10log(N_{st} - 1)$. In this particular design, we chose $N_{st} = 6$, and 8-bits, setting an upper limit for rejection around 50 dB.

2. Tradeoffs of the Transmission Line

The two main parameters that define the frequency range of the distributed transmitter are the inter-stage delay of the TL, τ_d, and the number of stages, N_{st}. Although, in theory, both perfect rejection and arbitrary output power can

be supported at all non-zero frequencies, the efficiency becomes unacceptable outside a certain range of frequencies. For frequency approaching $1/(2\tau_d)$ at the high end and below $1/(4N_{st}\tau_d)$ at the low end, efficiency becomes significantly degraded, making reasonable operation unfeasible. Thus N_{st} sets the range of frequencies that are reachable as $f_{max}/f_{in} \approx 2N_{st}$, while the per-stage delay τ_d sets the upper frequency limit. Other limits on performance include the loss from inductors and capacitors, TL cutoff frequency, and the finite output impedance of the individual PAs. As diagrammed in Fig. 2, the system can be modeled as alternating series inductors and shunt capacitors, with loss associated with inductors modelled as series resistance $R_S = L\omega/Q$. It can be shown that the total loss from R_S is equal to $N_{st}\ \tau_d\omega/Q$, favoring a shorter TL. Each sub-transmitter is modelled as a controlled transadmittance in parallel with output resistance R_{out} and capacitance C. While the output capacitance of the sub-transmitters can be absorbed into the TL itself, the output resistance is lossy, which we address with PA degeneration.

4.2.2 RX-Tracking PA Degeneration

The noise coming from the shared baseband circuits are correlated and filtered, and, similarly, the TX and RX LO noise sources are also correlated and therefore, are suppressed by the distributed suppression. However, the noise generated by the sub-transmitters themselves is not correlated and therefore cannot be suppressed by the distributed duplexing that cancels the correlated TX signals at the RX port. The uncorrelated noise comes from both the common source stage of the PA itself, ($\overline{i_n^2} = 4kT\gamma g_{m,PA}$), and from preceding RF and baseband circuits ($\overline{i_n^2} = \overline{v_{n,TX}^2} g_{m,PA}^2$), where $\overline{v_{n,TX}^2}$ is the noise of all TX stages before the PA.

Noise from the combined N_{st} sub-transmitters will therefore degrade the NF at the RX port by at least:

$$NF > 10log(1 + \gamma N_{st} A_v + N_{st} \frac{\overline{v_{n,TX}^2} A_v^2}{4kTR_L} \tag{4.4}$$

where $A_v = g_{m,PA} R_L$ is the voltage gain of a single PA, and R_L is the parallel impedance of the two ends of the TL, typically 25Ω. Thus, for a composite voltage gain of $V_{out}/V_{in,TX} \approx 10$, $NF > 10dB$ just from the PAs themselves, excluding all other noise sources.

Because this noise is intrinsically related to the gain of the transmitter, it cannot simply be suppressed through careful design of standard transmitter circuits. Preventing this noise from desensitizing the receiver without destroying transmitter function requires selectively suppressing the PAs' gain in the RX band relative to the TX band.

To suppress the transmitter's noise and boost its output impedance in the RX band, we employ a passive mixer-based PA degeneration scheme to provide a high, narrow-band degeneration impedance at the RX frequency, as shown in Fig. . A passive mixer is connected to the source of each PA's common source device, in parallel with a large-value DC choke for bias current. The mixer's baseband port is loaded by large capacitors, and its LO port is driven by the RX local oscillator (LO) signal of frequency ω_{RX}.

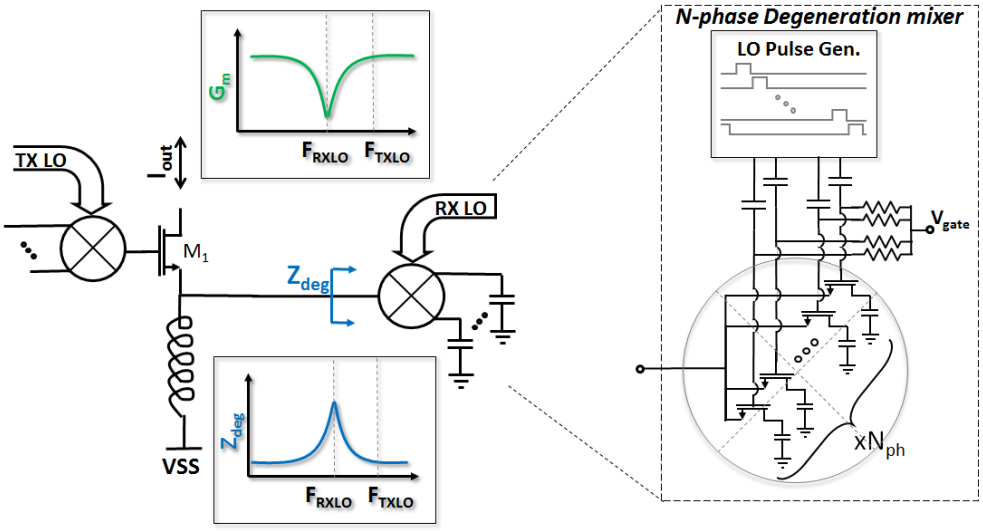


Figure 4.3: RX-tracking PA degeneration. Left: concept, common source amplifier (M_1) is degenerated by an inductor in parallel with a passive mixer. The mixer is a high impedance near $f_{RX,LO}$, but low elsewhere, including $f_{TX,LO}$. The effective transconductance of the amplifier is notched at $f_{RX,LO}$. Right: implementation of N_{ph} phase mixer with LO pulses AC-coupled to gates.

From [59] an N_{mix}-phase passive mixer presents a band-pass impedance centered at ω_{RX} is :

$$Z_{deg} = R_{sw} + \frac{R_{sw} + R_{sc}}{1 - sinc^2(\pi/N_{mix})} || \frac{sinc^2(\pi/N_{mix})}{j|\omega_{in} - \omega_{RX}|C_L N_{mix}} \tag{4.5}$$

Here, R_{sw} is the on resistance of the passive mixer switches, and R_{sc} is the source impedance looking out of the passive mixer's RF port, or roughly $1/g_{m1}$. Analysis of Eq. 4.5 shows that when $|\omega_{in} - \omega_{RX}| \gg 0$, the input impedance of the degeneration mixer $Z_{deg} = R_{sw}$. But when $\omega_{in} \approx \omega_{RX}$, the input impedance in RX band increases to:

$$Z_{deg}(\omega_{RX}) = R_{sw} + \frac{R_{sw} + R_{sc}}{1 - sinc^2(\frac{\pi}{N_{mix}})} \tag{4.6}$$

The composite transconductance of the PA is reduced Z_{deg} to be $G_{m,PA} = \frac{g_{m1}}{g_{m1} Z_{deg}(\omega)}$, so that the band-pass degeneration impedance produces a band-notch

PA transconductance, as shown in Fig. 4.3. Substituting Z_{deg} from Eq. 4.6, and assuming that $|\omega_{TX} - \omega_{RX}| \gg (R_{sw} + g_{m1})N_{mix}C_L$ the relative amount of degeneration between RX and TX bands is:

$$A_{deg} = \frac{G_{m,PA}(\omega_{RX})}{G_{m,PA}(\omega_{TX})} \approx (1 - sinc^2(\pi/N_{mix})) \tag{4.7}$$

For an 8-phase mixer ($N_{mix} = 8$, this implies an ideal $A_{deg} \approx 1/19.8 \approx -26dB$. Since gain terms A_v are reduced by this factor of A_{deg}, the RX-band NF is substantially reduced with much less impact on TX-band gain.

This degeneration technique also increases the output impedance of the sub-transmitter PAs' R_{out} by a factor of $1/A_{deg}$ in the RX band. Since $R_{out}(\omega_{RX}$ acts as a shunt loss mechanism, attenuating incoming RX signals by $-N_{st}20log(1 + R_L/R_{out}(\omega_{RX})$ dB, increasing R_{out} by $1/A_{deg}$, greatly mitigates shunting RX loss.

4.2.3 Impact of Techniques Various Noise Mechanisms

Although the techniques proposed above mitigate noise degradation of the RX by the TX, careful design of the various sub-blocks shown in Fig. 4.4 is still required to avoid excessive RX-band noise from the various TX elements.

TX noise sources in this design are subject to one or more of the following mitigating mechanisms:

1. Any noise mechanism introduced in the transmitter before upconversion will be subject to at least one pole of low-pass filtering in the TX baseband, suppressing it in the RX band.

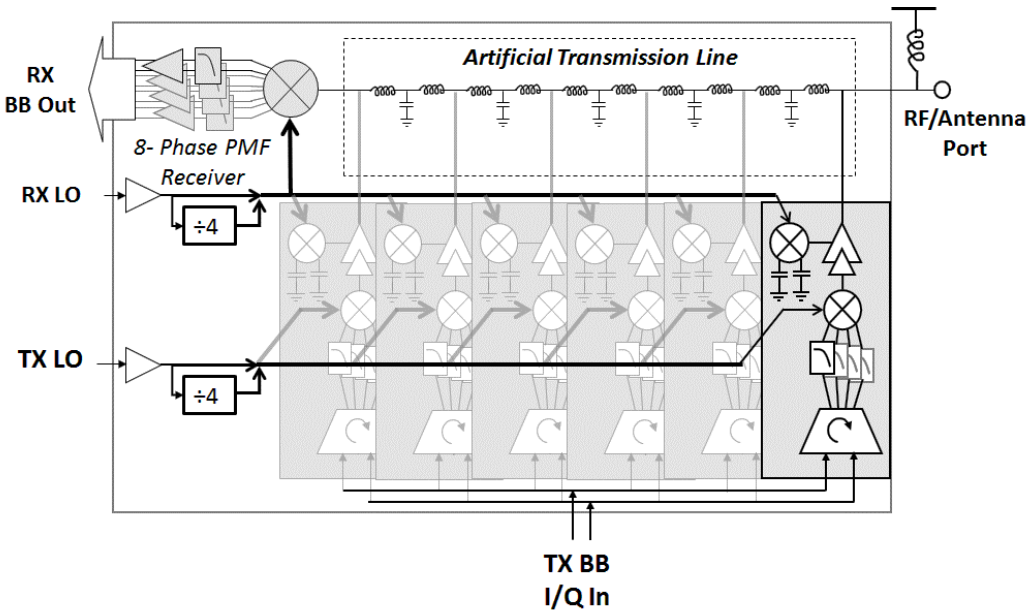


Figure 4.4: System block diagram. TX LO and baseband signals are distributed to six sub-transmitters, each with independent complex gain, upconversion and degenerated PA. TX cells are coupled into LC passive delay line, connecting the antenna port and receiver. The RX LO is distributed to the receiver and TX degeneration mixers.

2. Any noise mechanism that maps to a voltage on the gate of the PA core device will be subject to the RX-LO tracking degeneration. This includes noise from baseband, upconversion and RF pre-amplification circuits, all suppressed by a factor of A_{deg}^2, and PA noise, suppressed by A_{deg}. It also includes phase noise present of the TX LO, suppressed by a factor of A_{deg}^2.

3. Finally, noise that is correlated across transmitters is suppressed by a factor $A_{dist} \approx (\omega - \omega_{TX})|/\omega_{TX}$, reflecting the fact that sub-TX gains are weighted to cancel at the RX port of the TL. This includes any noise present on the TX baseband inputs (from DAC quantization noise, for example). It also includes the LO phase noise common to all 6 transmitters. This applies not just to the TX LO phase noise, but also to the RX LO phase noise. Phase noise in the RX LO, at the TX frequency, acts through the

degeneration mixers to downconvert the TX signal to near DC. The mixers then re-upconvert this signal into the RX band, generating RX-band noise proportional to the TX signal and RX LO phase noise. But this noise is correlated across sub-transmitters and proportional to sub-TX signals' magnitude and phase, so it is suppressed similarly to the TX signal. These concepts are explained in much greater detail in Chapter 5.

4.3 Circuit and Subsystem Design

The full system is shown in Fig. 4.4. A six-stage distributed transmitter was implemented with 5 TL segments. Each sub-transmitter (detail in Fig. 4.5), comprises a 1-quadrant baseband rotator followed by a 4-to-8 phase interpolator, a 45-degree-resolution 4-quadrant rotator, 8-phase passive upconversion mixer, RF pre-amplifier, and degenerated PA. Up-conversion and degeneration mixers are driven by shared LO signals. These shared LO signals are generated by global RX and TX LO blocks and are locally retimed (further explained at subsection E) at each sub-transmitter. The RX LO also drives the RX down conversion mixer.

Because signal level builds up along the TL, as illustrated in Fig. 4.1, PAs close to the receiver see much smaller signal swings than those close to the antenna port. Ideally, the supply rails would be stepped up linearly along the length of the TL in proportion to the signal level to maximize system efficiency. In this design, we compromised with two VSS supply rails (GND and VSS PA) as shown in Fig. 4.6, eliminating 50% of the wasted power lost in a single sup-

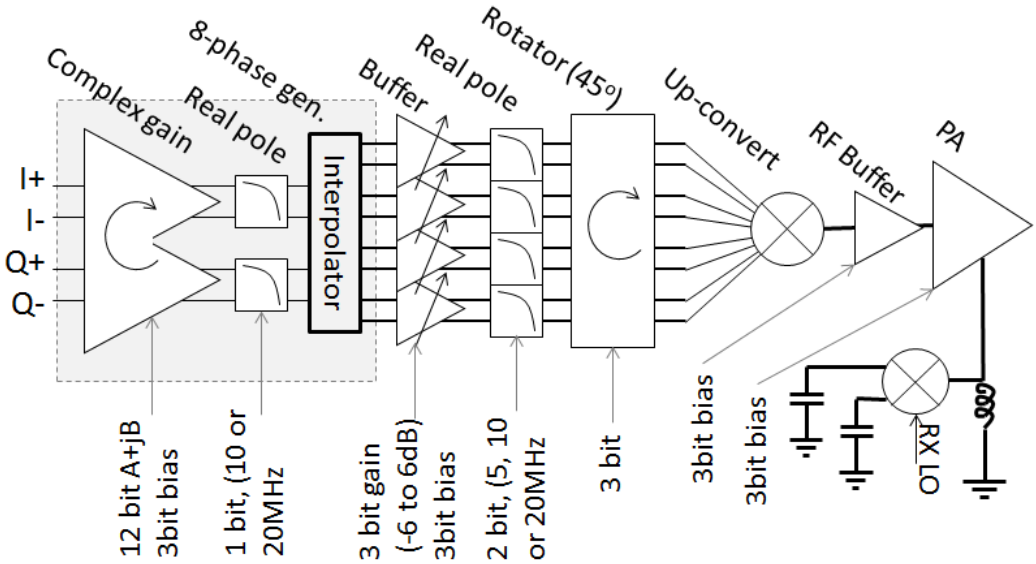


Figure 4.5: Detail of sub-transmitter design, showing controls for gain, bandwidth, rotation angle and current bias.

ply design. In future designs, this was upgraded to a more dynamic scheme (see Chapter 6).

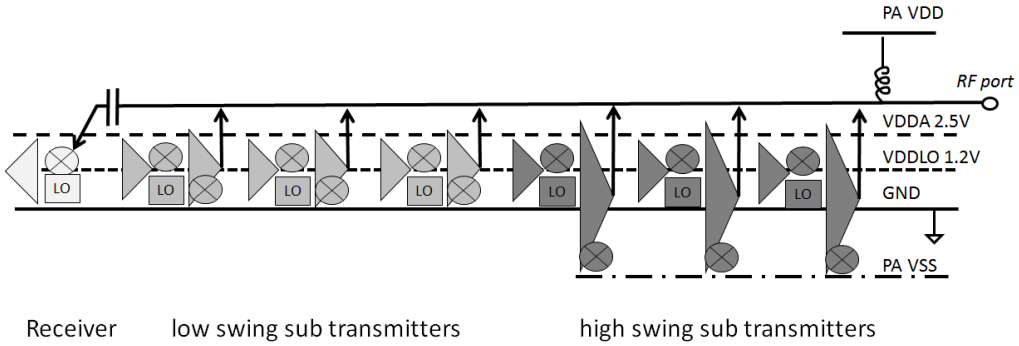


Figure 4.6: Power supply distribution: LO and Analog circuits were supplied by 1.2 V and 2.5 V respectively. High swing PAs were supplied with a VSS below GND (-2.5 V), and the main transmission line was biased through an off-chip choke to the PA VDD (2.5 V).

4.3.1 Complex-Weighted Programmable TX Baseband

The TX baseband starts with an interpolator, as in Fig. 4.5 and in more detail, Fig. 4.7, to combine the I and Q inputs so that $I_{out} = AV_I + BV_Q = Mcos(\omega_{BB}t + \theta)$. With the correct choice of A and B, implemented by binary-weighted programmable input differential pairs as shown in Fig. 4.7a, an output with constant amplitude and a specific phase between 0° and 90° can be generated.

A resistor network is added to further interpolate the 4-phases to 8-phases with 45-degree phase splitting. By choosing the resistor values correctly, as shown in Fig. 4.7b, this interpolating load provides matched output resistances and signal amplitudes at all 8 output ports. Note that this circuit operates similar to a harmonic rejection circuit, so that errors in resistor ratios result in unwanted 3rd-harmonic upconversion proportional to the magnitude of the error. A capacitive load filters all 8 outputs for noise. The first two stages generate programmable phase delay between 0 and 90 while phase shifts from 0 and 360 is required. Fortunately, the 8-phase signals inherently provide 45 phase splits and so after a second round of buffering and filtering, eight 8:1 analog MUXes were used to map the 8 baseband outputs to the 8 inputs of the upconversion mixer, providing an arbitrary phase shift by any multiple of 45.

4.3.2 TX RF Circuits: Upconversion, Preamplifier, PA

Once the TX baseband signals are weighted, filtered and interpolated to 8 phases, they must be upconverted independently in each sub-transmitter. An 8-phase passive mixer upconverts the signal, both to take advantage of low noise

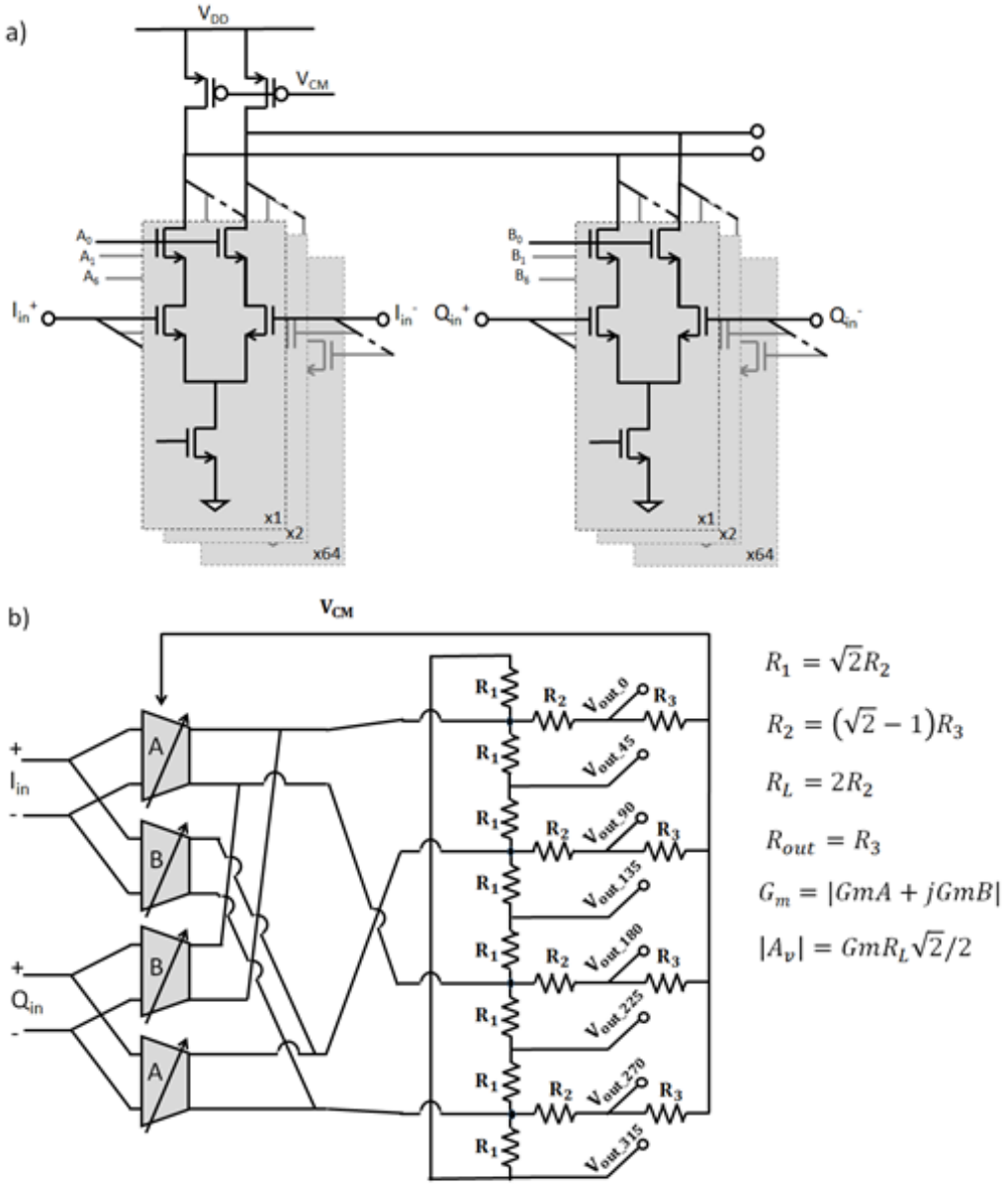


Figure 4.7: Interpolator: a) 1-quadrant I-Q interpolator: banks of unit differential pairs provide real and imaginary transconductance terms with magnitudes A and B. b) A 4-to-8 phase interpolating resistive network, with the given values for R_1, R_1 and R_1, presents a differential load to the I and Q transconductance from (a) and generates equal magnitude, 45° rotated output voltages each with output resistance $R_{out,BB}$.

of such structures, and to suppress up-conversion to the 2nd through 6th harmonics.

One downside to this approach is the limited signal amplitude that passive mixers can support. This small signal swing requires inclusion of an RF pre-amplifier before the output (PA) stage. The pre-amplifier is a simple, resistively loaded common-source amplifier with a gain of 2.5 (8dB) and output swing up to $2V_{pp}$. The expected output noise of the mixer and pre-amplifier must be kept low to avoid desensitizing the receiver, even when suppressed by A_{deg}^2. $R_{sw,mix}$ was designed to be $\sim 7\Omega$, $R_{L,pre} = 20\Omega$ and so $g_{m,pre} = 125mS$.

The output stages ("PAs", shown in Fig. 8) of each sub-transmitter achieve several conflicting goals at once. The first is to provide stand-alone voltage gain with low noise. Each stage achieves a voltage gain of approximately $2\times$ (6dB), so as to provide a composite voltage gain across all 6 stages of about $10\times$, accounting for TL loss. Since the TX line presents a load of 25Ω to the PA (50Ω from each side), this requires a transconductance of $G_{m,PA} = 80mS$ from the amplifier. This $G_{m,PA}$ includes the on resistance of the degeneration mixer, designed to be $\sim 7\Omega$. As a result, the transistor g_m needs to be close to $200mS$ to achieve the desired overall $G_{m,PA}$.

Beyond gain and noise, the PA is also designed for high output impedance, since low R_{out} in a distributed amplifier adds shunt loss paths to the TL. Likewise, the individual PAs must withstand large swing on their outputs without their gate oxide breaking down. Therefore, we employed a stacked cascode structure: a single cascode was used in the three PAs closer to the RX, a double cascode for those closer to the antenna where both supply voltage and signal swing are larger. Overvoltage between the drain and gate is mitigated by combining a resistive bias ladder to bias the cascode devices with a capacitive cou-

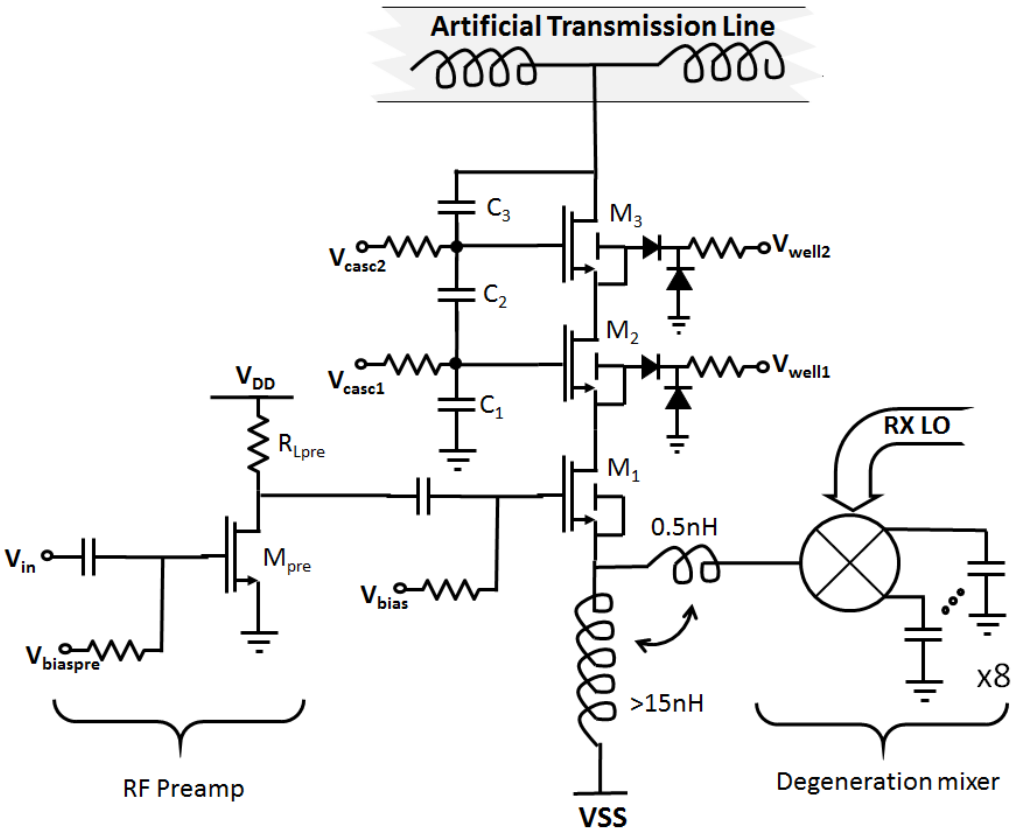


Figure 4.8: PA, Pre-amp and degeneration circuit design. The RF preamp boosts the output of the upconversion mixer. The PA consists of a replica-biased common-source amplifier, with one or two cascodes. The cascode gates are biased to distribute the supply voltage across the transistors drain-gate junctions, avoiding breakdown. $C_1 - C_3$, ensure that output signal voltage is also evenly distributed. Triple-well devices are used for isolation, with the p-well (body) connected to source, and nwells biased similarly to gates.

pling network tied to the drain of each PA as shown in Fig. 8. This allows the gates to move in an AC sense and significantly reduce the swing across the gate drain junction at a small cost in gain and output impedance.

We used triple-well devices for PA devices, as well as all mixer switches. For PAs, we tied p-bulk to the source and the deep-nwell to ground (for the input device and mixers) or a resistive ladder (for the cascodes) so that junctions stayed reversed biased and reverse bias never exceeded 3.5V, even when VSS

was pulled below ground. For ESD on the PA source node, we have a diode to ground to protect against positive excursions, and the PA itself should self-protect against moderate negative ESD excursions.

4.3.3 Artificial Transmission Line Design

The TL is composed of series-L/shunt-C sections, integrated on-chip, where $L = 2nH$ and $C = 800fF$, to provide the desired 50Ω characteristic impedance and a broadband impedance match. We use MIM capacitors on intermediate segments, and the PA's parasitic drain capacitance as the capacitor to ground on PA-driven segments. Two LC sections per stage were found to provide sufficient delay ($80ps$) while keeping the intrinsic cutoff frequency $1/\sqrt{LC}$ above 4GHz, this was chosen to ensure high-frequency performance was not limited by the TL, and so represents factor-of-2 over-design for the frequency range we achieved. Simulations indicate that for these choices, the system should ideally maintain $\sim$40 dB of rejection for $\pm$10 MHz BW around center frequencies from 500 MHz to 3 GHz. Our on-chip inductors were simulated to achieve $Q > 10$ across the frequency range of interest.

4.3.4 Degeneration Design

The RX-tracking degeneration consists of two elements (as shown in Fig. 4.7): a passive mixer to provide a narrow-band high impedance at the RX frequency, and a parallel choke inductor to provide a DC path for the PA's bias current. This inductance need not be high-Q, allowing a relatively high value on-chip in-

ductance of 10-15 nH ($10nH$ @500 MHz, $15nH$ @2.5 GHz) with a DC resistance of about 8Ω, for a 250 mV DC drop at maximum bias current. The degeneration choke inductor of each sub-PA is connected directly to its own bond-pad to take advantage of additional bond wire, package, and board-level inductance.

With an 8-phase passive mixer, one would ideally see a degeneration impedance roughly 19.8 times the out-of-band impedance (see Section 4.2.2). Practically, however, this ratio assumes a broadband impedance presented to the mixer which is constant even at higher (7th, 9th, etc.) harmonics of the RX LO frequency. Parasitic capacitance on the RF port will act to shunt harmonics, reducing this ratio [60]. By including a small (~ 500 pH) series inductance, the impedance at the harmonics is boosted, enhancing A_{deg} [61]. Even further enhancement was achieved by co-winding this low-value high-Q inductor with the high value, low-Q choke inductor, providing a combined improvement of 2-3 dB. Simulations indicated that this composite degeneration structure provided a 14dB notch in noise coming from the PA in the RX band compared to out-of-band (see Fig. 4.9).

4.3.5 LO Line Distribution

8-phase passive mixers require 12.5% duty-cycle LO pulses [60, 25] with a fixed phase relationship to ensure the desired performance. The LO signals should also have low, correlated phase noise to take maximum advantage of the suppression of correlated noise at the receiver port. The 6 sub-transmitters therefore need to share two common LOs (one for upconversion at $_{TX}$ and one for degeneration at $_{RX}$). However, 12.5% duty-cycle, sub-1ns pulses, if distributed across circuits that are millimeters apart will be badly degraded due to dispersion in

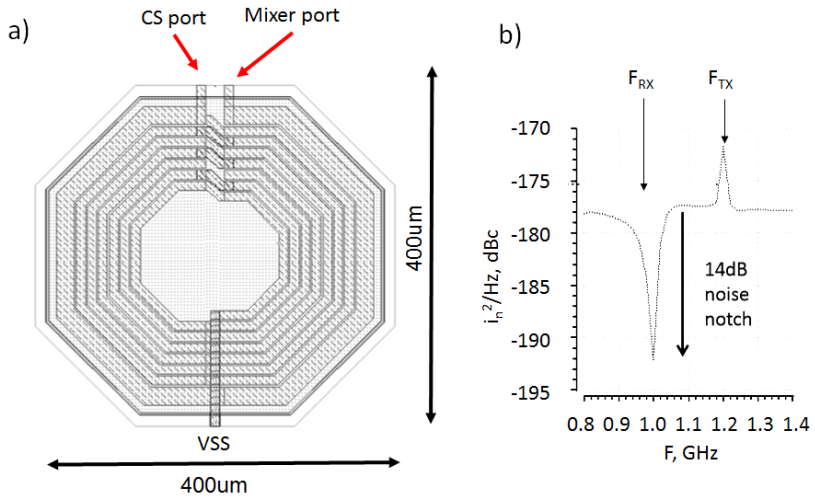


Figure 4.9: Degeneration details: a) layout of choke inductor and mutual mixer inductor. b) PSS simulation showing 14 dB enhancement of PA noise with mixer-based degeneration.

the wires [59].

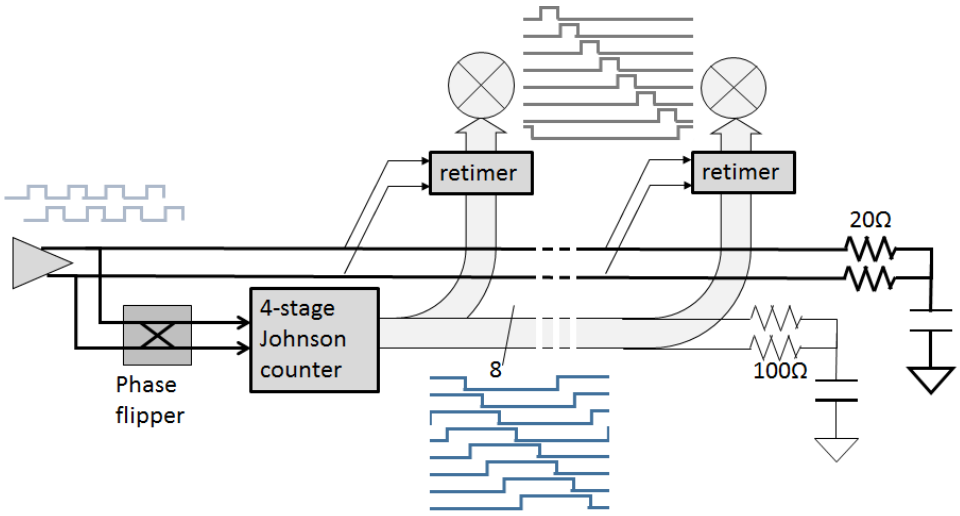
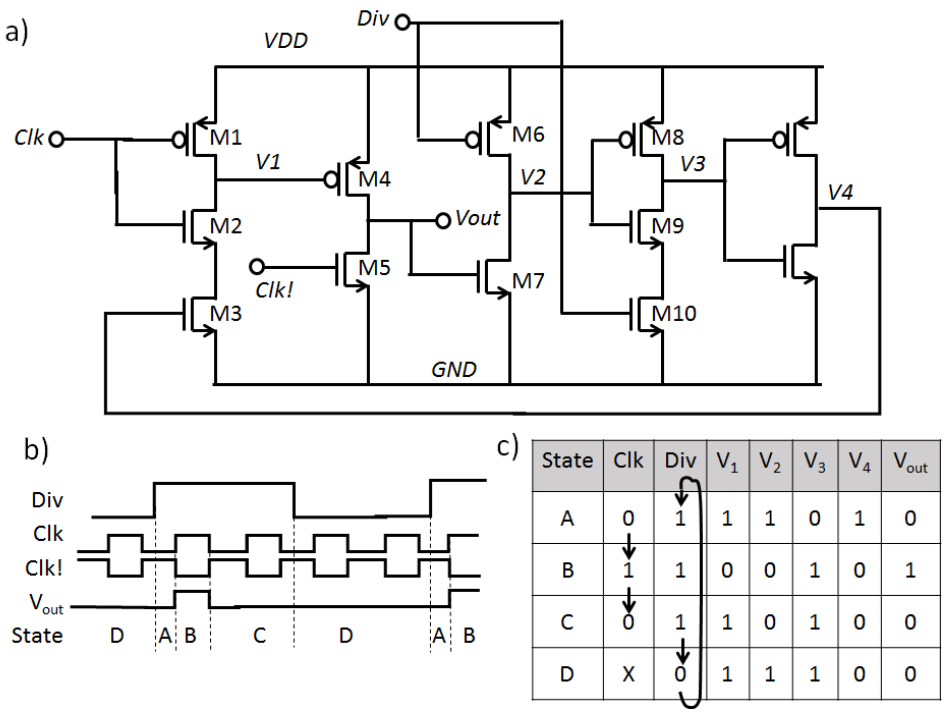


Figure 4.10: Distributed LO system. Differential 4X LO signals (*clk*) are buffered, and drive a 4-stage Johnson counter to generate 8, 45-degree-split square waves. These 10 signals are distributed to local retime circuits in each sub-transmitter to generate 12.5% duty-cycle LO pulses. A "phase flipper" allows shifting of divided down signal to avoid race conditions in the retimers.

In order to avoid distributing 12.5% duty cycle LO signals across the chip, we

instead generated 45° phase-split 50% duty-cycle signals from a shared Johnson counter, and then distributed those signals and the original LO signals to retimer circuitry in each sub-transmitter, as shown in Fig. 4.10. The retimer is a state machine in dynamic CMOS logic, as shown in Fig. 4.11. Briefly, each retimer receives a phase-split divider output *div*, whose rising edge puts the circuit in a sensitive state. The output of the retime (which drives one mixer switch's gate) then rises with the next rising edge of *clk*, the 4X LO signal, and falls with the next falling edge of *clk* (also the rising edge of *clk*). After this single pulse, the output stays low until reset by the falling and subsequent rising edges of *clk*, generating a 12.5% duty cycle pulse with the same relative phase and frequency as *div*.

This approach provides several benefits: **1)** the precise timing of the edges



State	Clk	Div	V_1	V_2	V_3	V_4	V_{out}
A	0	1	1	1	0	1	0
B	1	1	0	0	1	0	1
C	0	1	1	0	1	0	0
D	X	0	1	1	1	0	0

Figure 4.11: Dynamic LO retime and pulse generator: **a)** transistor-level circuit of pulse generation state machine, only M1-M5 contribute to phase noise. **b)** Timing diagram showing sequence of 4 states, V_{out} and critical edges of clk and div. **c)** Internal voltages in each state.

of the output pulse depend only on the timing (and phase noise) of the 4X frequency LO signals; **2)** function is insensitive to the precise relative timing of clk and div except for a race condition at certain frequencies, which are resolved by a "sign flip" control on clk and $\overline{clk}$ (see Fig. 10); **3)** only a few transistors buffer clk to the output, so only these transistors must be sized for low noise. **4)** distributed LO signals are 50% duty cycle, making the circuit resistant to dispersion in their distribution across sub-transmitters. The long LO distribution lines were terminated by physical resistors to prevent undesired reflections.

4.3.6 Receiver Design

The receiver is similar to that reported in [25] but with the new LO retiming scheme described above. It provides an 8-phase output from 4 differential amplifiers, driven by the 8 output phases of the downconversion mixer, loaded by 8 large, programmable capacitors to ground. Gain, bandwidth and feedback impedance are programmable. Circuitry is included to modulate and cancel LO leakage at the RF port as in [62].

4.4 Measurement Results

The transceiver was fabricated in a 65nm CMOS process, and measures 2.4mm$\times$3.0mm, as in Fig. 124.12. It operates across a wide frequency range of more than 0.3-1.6 GHz. The system in the higher frequencies is limited by the LO performance generating 8 non-overlapping 12.5% duty cycle pulses becomes more challenging as the frequencies increase. Faster dividers and pulse

generators, especially with decreasing feature size should extend this range. The transceiver consumes 2.2 W while transmitting 16 dBm at 900 MHz and receiving at 785 MHz. The PAs consume a total of 600 mW from a 2.5V VDD and -2.5V VSS. The LO circuits, due to noise requirements, consume a total of 800 mW from a 1.2V supply, and the TX baseband circuitry and RF pre-amplifiers consume 700 mW from a 2.5V supply.

The RX baseband, consumes less than 100 mW from 2.5V. An unexpected (and unmodeled) flaw in which the n-well of the deep-n-well mixer switches were connected to GND instead of VDD prevented raising the bulk voltage above 0.6V. Since the gate and bulk voltages were referenced from the same source, the gate bias was lowered. This flaw limited the overdrive on the RX downconversion and TX upconversion mixers gates, significantly increasing their on resistance, degrading noise, linearity and signal amplitude.

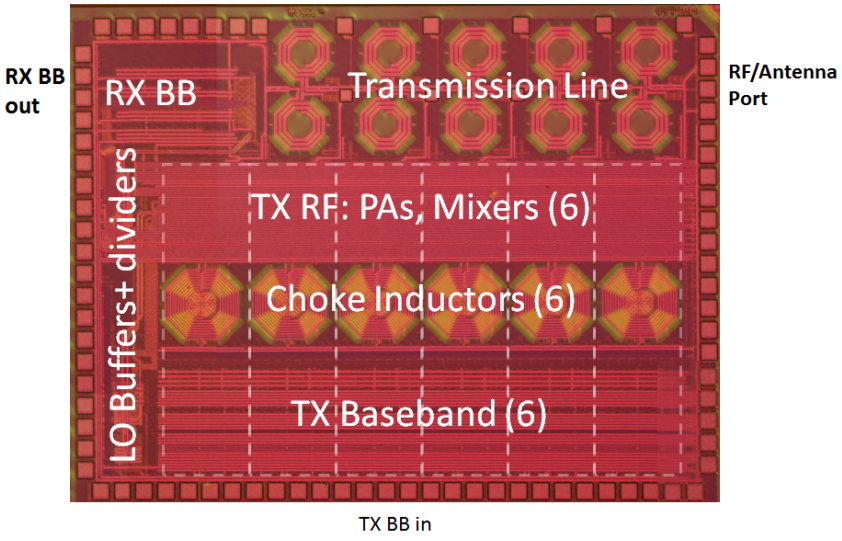


Figure 4.12: Die photo. The chip measures 2.4mm×3.0mm.

4.4.1 Basic Receiver Performance

As shown in Fig. 4.13, the receiver gain was between 24 dB and 32 dB over the range 200 MHz-1.7 GHz. At 8-12 dB, the RX NF (in Fig. 4.14) was 4-5 dB worse than expected from simulation and previous work [58] even accounting for the loss of the TL, (about 1.5 dB at 700 MHz). A 0dBm blocker at 700 MHz for a 600 MHz receive signal compressed the receiver by about 3dB, as shown in Fig. 4.15. Again, this is worse than expected: the degraded noise and linearity are both likely due to the underdrive of the mixer and associated a much higher R_{sw} value [60].

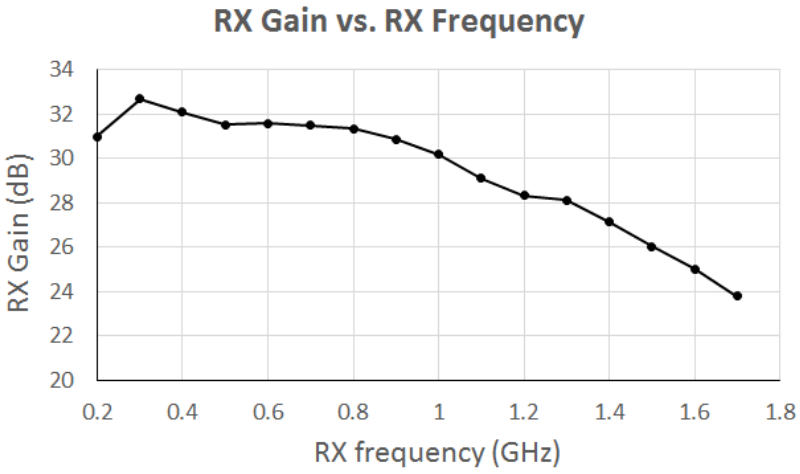


Figure 4.13: Measured RX gain across frequency.

4.4.2 Duplexing Performance

In TDD transmit mode (sub-TXs weighted to protect the receiver, but RX tracking degeneration mixer switches all turned on for minimum resistance), the transceiver reaches a peak output level of 19.5 dBm and 18% PA drain efficiency. The output level was >14 dBm across the 0.3-1.6 GHz range, with >25 dB of TX

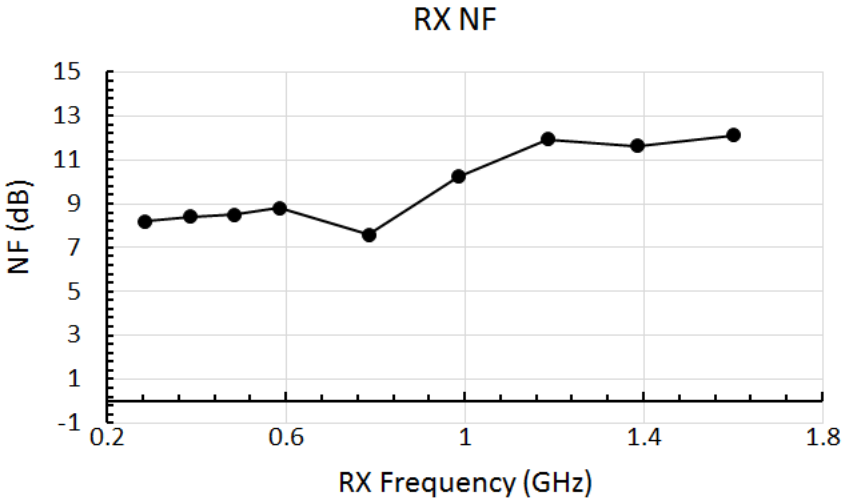


Figure 4.14: Measured RX NF across frequency.

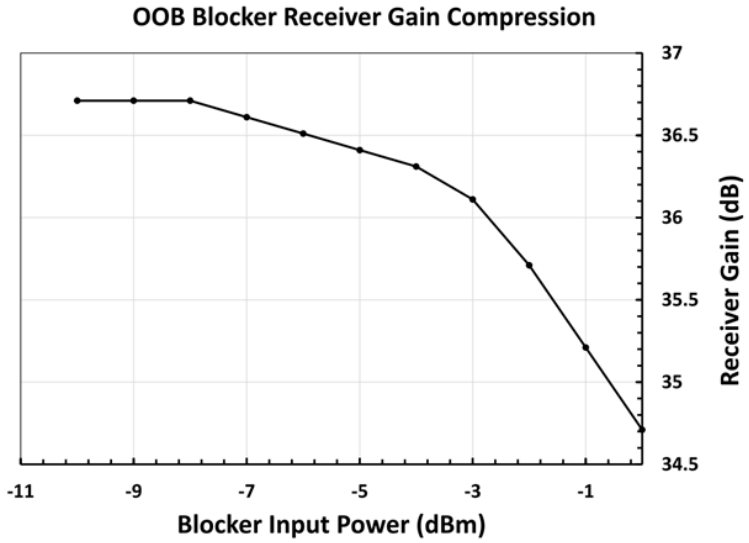


Figure 4.15: Measured out of band blocker induced RX gain compression.

suppression at RX (see Fig. 4.16). Signal levels were likely limited by under drive in the upconversion mixers, rather than the PAs themselves.

Since many duplexers' isolation is sensitive to antenna impedance, we explored the effects of changing VSWR. As shown in Fig. 4.17, we changed

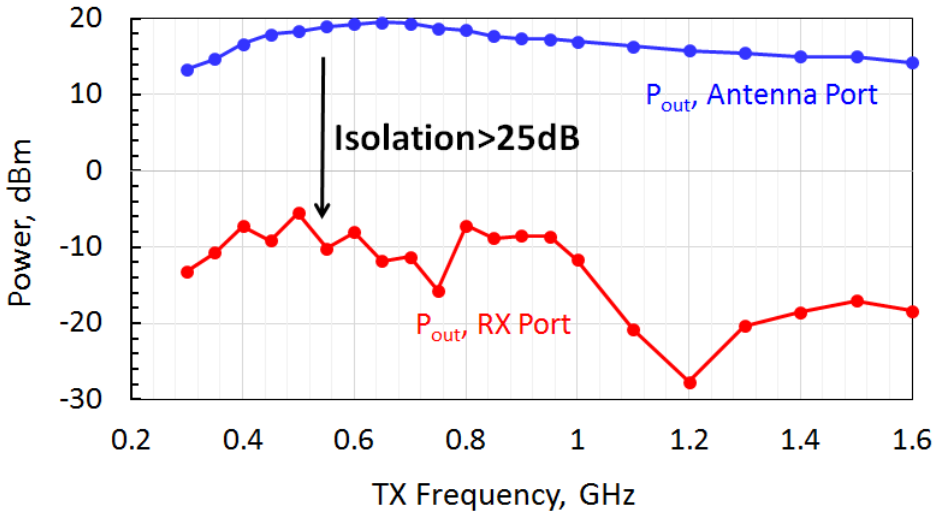


Figure 4.16: TX power at antenna port and RX port across frequency, degeneration OFF.

the RF port impedance for a 3:1 VSWR. This degraded the RX isolation by about 20dB, and the output power by 5.4dB. Re-computing the weights for the new impedance, recovered 2dB in P_{out}, and fully restored TX-RX isolation. TX-induced RX compression also recovered dramatically from re-calibration of weights.

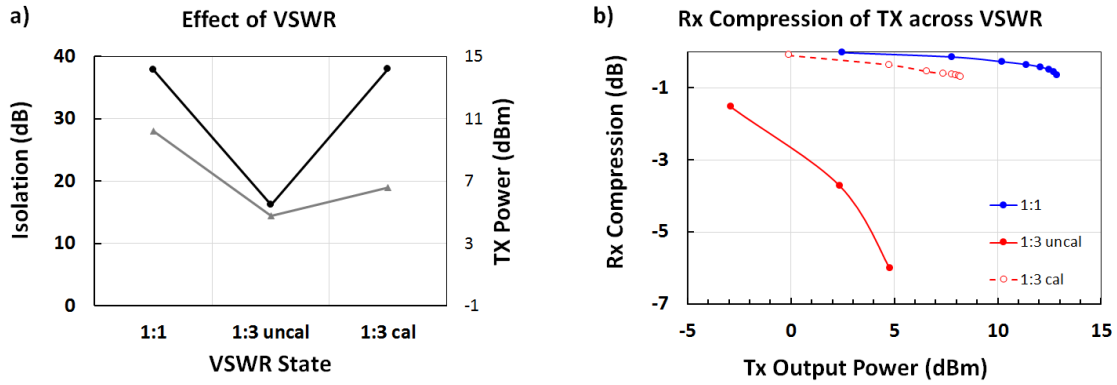


Figure 4.17: TX power at antenna port and RX port across frequency, degeneration OFF.

TX-RX isolation was moderately sensitive to nonlinear effects, especially at lower frequencies. Optimizing weights for P_{out} at -3dB back-off, and then in-

creasing to maximum P_{out} degraded TX-RX isolation by less than 8dB and for frequencies of 600MHz and above isolation stayed above 20dB, and could be retuned to better than 25dB with a slight adjustment to the weights.

4.4.3 Degeneration Performance

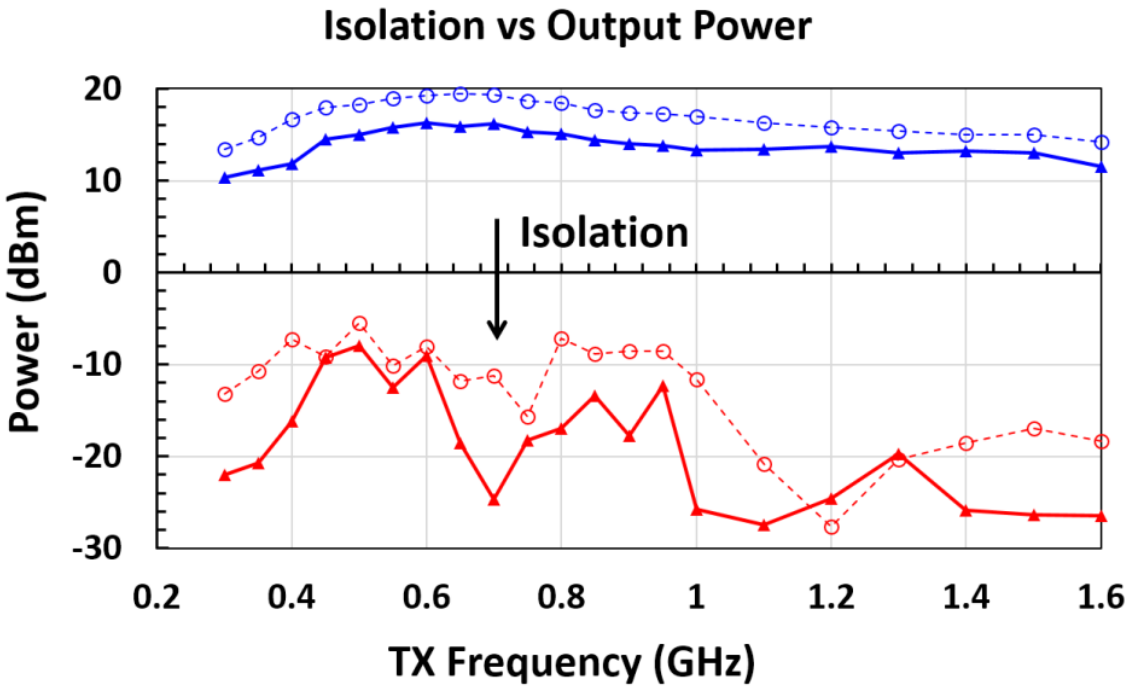


Figure 4.18: Effect of RX-tracking degeneration on TX power at antenna port and RX port across frequency, degeneration on (solid) or off (dashed).

As seen in Fig. 4.18, activating degeneration in the PAs reduced PA output power by 3-4 dB, but had little effect on isolation. To confirm the narrow-band effect of RX-tracking degeneration on $G_{m,PA}$, we injected a small TX input signal, and measured the output level as we swept $_{RX}$ relative to $_{TX}$ either with the degeneration mixer switches all on (inactivating the degeneration effect) or acting as an 8-phase mixer. Fig. 4.19 shows gain reduction across the band by

$\sim$4 dB, with further suppression by $>$9dB for $_{RX}$ close to $_{TX}$. We also confirmed degenerations impact on noise and shunting loss by comparing RX NF and gain when degeneration was on and off, across TX signal strength. As can be seen in Fig. 4.20 and Fig. 4.21, degeneration impacted NF by $>$13dB, and gain by 1.5dB.

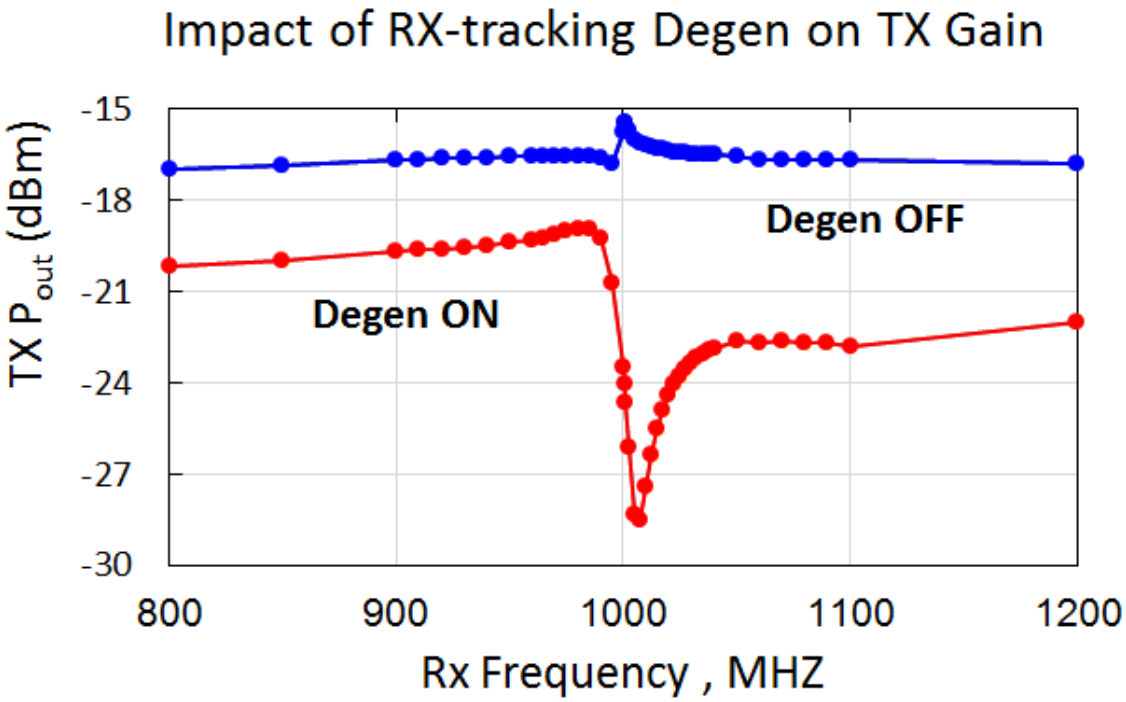


Figure 4.19: Effect of RX-tracking degeneration on TX power as a function of frequency separation.

Finally, we measured RX NF from 185-1615MHz under three conditions: with TX off, with TX on at moderate power and TX on with maximum output power. Degeneration was activated when the TX was on, and our results are shown in Fig. 4.22. With the TX off, the RX NF was 8-12dB. In simulation the NF is much less. We see of 3-4dB from the receiver and 0.5dB from the transmission line. We attribute the discrepancy to the design flaw described earlier, causing an overall increase of 5-8dB. However, when the transmitter was fully biased, NF degraded by about 4-5dB due to TX noise being injected into

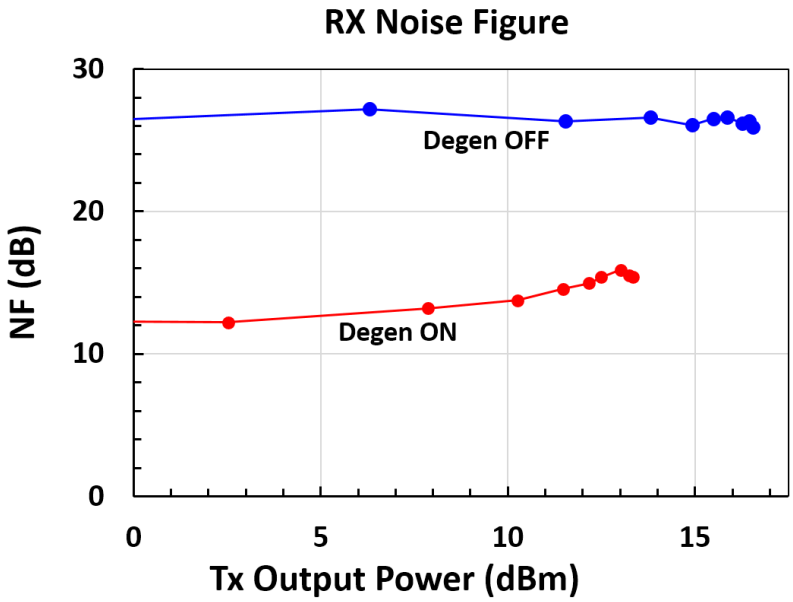


Figure 4.20: Effect of RX-tracking degeneration on RX NF vs TX P_{out}. f_{TX}=1GHz, f_{RX}=885MHz.

the RX band. Degradation due to this mechanism was worse at band edges. At high frequencies, the degeneration circuit likely underperformed due to reduced swing of the LO, and at low frequencies, AC-coupling degraded LO amplitude, while the degeneration choke inductor's impedance was low enough to shunt the impedance presented by the degeneration mixer. At maximum TX power, NF was degraded by an additional 2-3 dB mid-band, but much more at the band edges. We attribute this additional degradation to the same reduced LO swing, with the added problem of the degeneration mixer becoming overloaded by large TX signals. Addressing this overload will be an important aspect of future work.

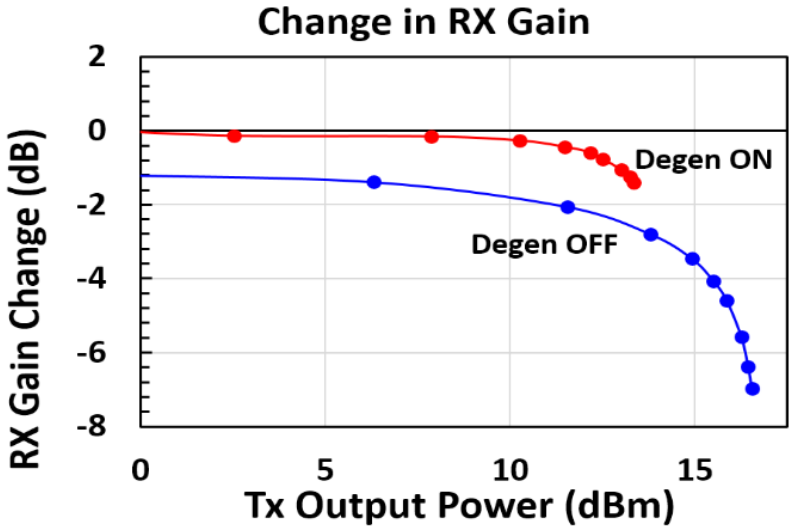


Figure 4.21: Measured effect of RX-tracking degeneration on RX gain across TX output power. f_{TX}=1GHz, f_{RX}=885MHz.

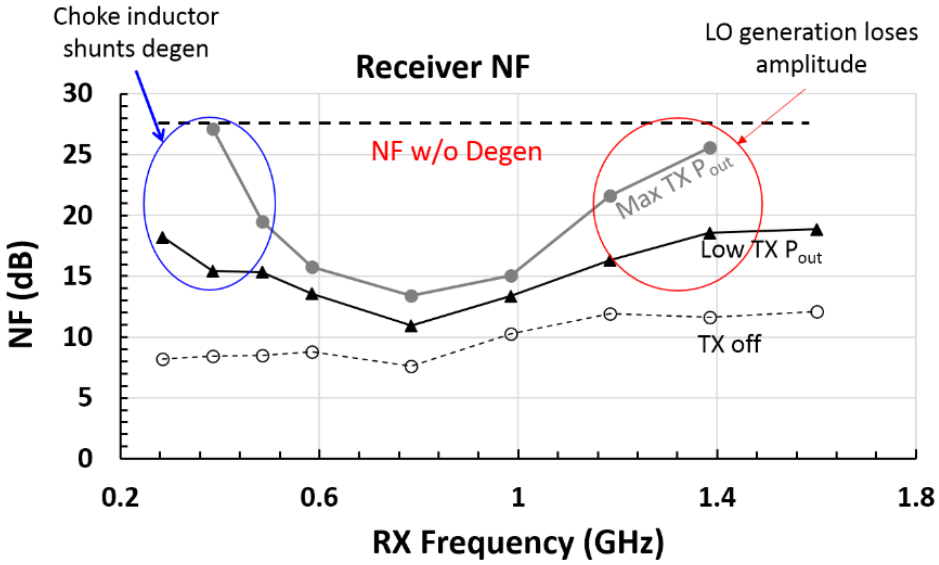


Figure 4.22: Measured effect of TX state on RX NF across frequency, for low and maximum output power. RX NF with TX off is shown for comparison.

Parameter	[46]	[52]	[54]	[55]	[56]	This Work
Technology	65nm	90nm	40nm	65nm	65nm	65nm
Duplex IL	2.9dB	2.9dB	2.9dB	2.5dB	4.4dB	0dB
Isolation	>20dB	>50dB	>50dB	>45dB	>49dB	30dB
RX NF	4.8dB	5.9dB	6.1dB	5.0dB	∼6dB	7dB
Frequency	0.8-1.4GHz	1.7-2.2GHz	1.5-2.4GHz	3G/4G	710-970MHz	0.3-1.5GHz

Table 4.1: Performance Comparison to the State of the Art

4.5 Conclusion

In this Chapter, we presented a new type of flexible, programmable transceiver that is capable of TDD and FDD with single antenna for RX and TX, across a tuning range of 0.3-1.6GHz. In TDD mode, the transmitter was able to achieve a transmit power level >19dBm. In FDD mode with active degeneration, TX power was as high as 15.5dBm with >25dB of TX-RX isolation. We discussed the methods to compute complex weights to achieve this isolation figure.

8-phase passive mixers were used for TX upconversion, RX downconversion and degeneration. The RX NF during FDD operation was degraded by only 4dB relative to the RX only NF as expected. While a design flaw means that performance of this prototype was slightly degraded relative to other approaches to integrated duplex (see Table 1), the presented approach provides a significantly wider tuning range while maintaining acceptable isolation, and has significant potential for further improvements.

This work also reveals several areas for further development, besides the obvious need to fix the flaw in the mixers. In particular, while this work clearly demonstrates the utility the adaptive distributed duplex, the approach here assumes a narrow band signal passing through a linear circuit. Future work must pursue circuits and algorithms that enable adaptation for wider-band signals

and enable distributed digital predistortion to account for non-uniform nonlinear effects across the transmitter stages. Some of these directions are explored in Chapter 6.

CHAPTER 5

BROADLY TUNABLE FDD TRANSCEIVER: THEORY AND OPERATION

As wireless data demands increase due to the proliferation of smartphones and other connected devices, it becomes critical to have solutions to enable better utilization of existing spectrum and whitespace. Duplexing is an important solution to this problem, but it is challenging due to self-interference which requires analog cancellation. Previously, we presented a novel duplexing, single antenna transceiver architecture that utilizes a N-stage distributed amplifier combined with a transmission line to achieve transmit-receive isolation. The structure also includes a frequency selective, passive mixer based sub-transmitter degeneration to reduce TX noise in the RX band. In this Chapter, we analyze the theoretical bounds of this structure and relate system parameters such as number of stages N to figures of merit such as isolation and efficiency. Finally, we analyze the mechanisms that contribute to receiver noise.

5.1 Introduction

As wireless data demands increase, scalable, fast, wideband and widely tunable wireless systems are becoming ever more necessary. The breadth of this problem requires a multifaceted solution: there is a trend towards making use of whitespace spectrum (e.g. unused satellite and TV bands) which requires the utilization of transceivers that can support a multitude of bands. Furthermore, existing spectrum can be used more efficiently with hardware that supports frequency division duplex (FDD) and full-duplex (FD) [8, 14, 9]. Furthermore, peer-to-peer FDD, while not as spectrally efficient as FD, has network level im-

plications in terms of relaying that improve total system capacity without being as costly as FD system. Both of these solutions have inherent challenges: the current state of the art multi-band FDD/FD systems use multiple antennas and/or multiple off chip duplexers which are costly and large.

Furthermore, while there has been a significant interest in integrated duplexers [6, 63, 64, 7] achieving both good isolation (>50dB) and high TX output power (>20dBm) over multiple octaves of center frequency has proven to be nontrivial. These challenges are exacerbated by the need for high DC-to-antenna TX power efficiency and low receiver noise figure. Recent work [64] has demonstrated a combination of techniques that can provide suppression of TX RF signals at the receiver, while also suppressing the noise injected by the TX and mitigating shunting loss caused by the transmitter output sharing an antenna interface. This system utilized a single antenna, and was tunable across multiple octaves.

In this Chapter, we provide a full theoretical analysis of the class of circuits that enable the multi-band, widely tunable, FDD capable, single antenna duplexing transceiver presented in [64], and shown in Fig. 5.1. Similar to [65] we analyze: **1.** The fundamental behavior of a distributed duplexing transceiver with multiple sub-transmitters each with independently controllable complex gain driving an artificial transmission line. **2.** Algorithms for selecting these complex weights to null the transmitter signal at the receiver while optimizing efficient transmission. **3.** Analysis of this combined circuit/algorithm design space in terms of weight precision, number of stages, frequency, and various circuit parameters. **4.** Analysis of N-path-based degeneration of common-source amplifiers, and its impact on gain and noise across frequency. **5.** Analysis of

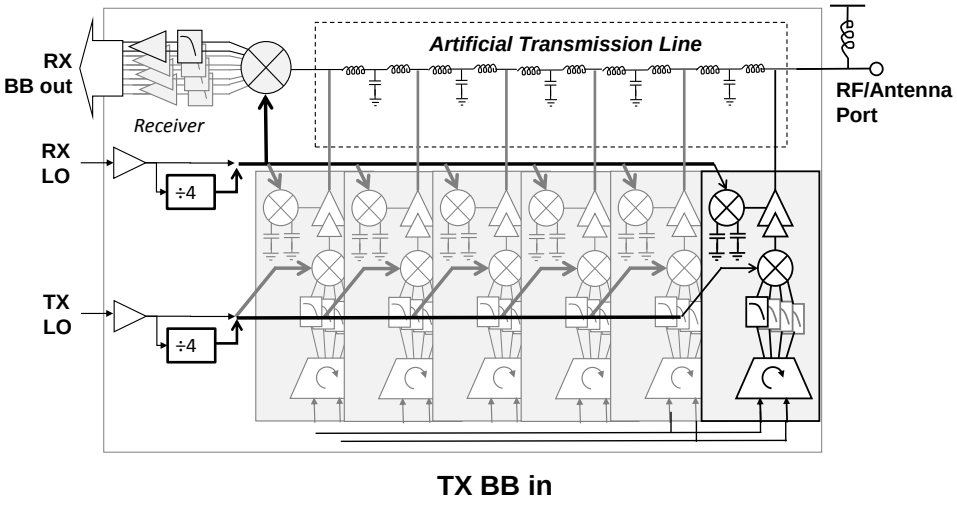


Figure 5.1: System architecture of a 6-stage transmission line based transceiver, with frequency selective degeneration.

the various noise contributors in a transmitter employing an N-path degenerated power amplifier, both alone and as part of the distributed architecture, described in parts 1-3. **6.** Specific analysis of the impact of different noise sources on RX and how they are affected by degeneration and distributed duplexing.

5.2 Distributed Duplexing: Circuits and Algorithms

5.2.1 Basic Two Tap Case

In this Section, we describe our design approach from top down by explaining specifically how striving for high isolation while maintaining high output power for a wide range of frequencies informed the design parameters of our system.

Begin by considering the 2-tap scenario shown in Fig. 5.2. In this structure, we have two sub-transmitters with phase and gain control at the input

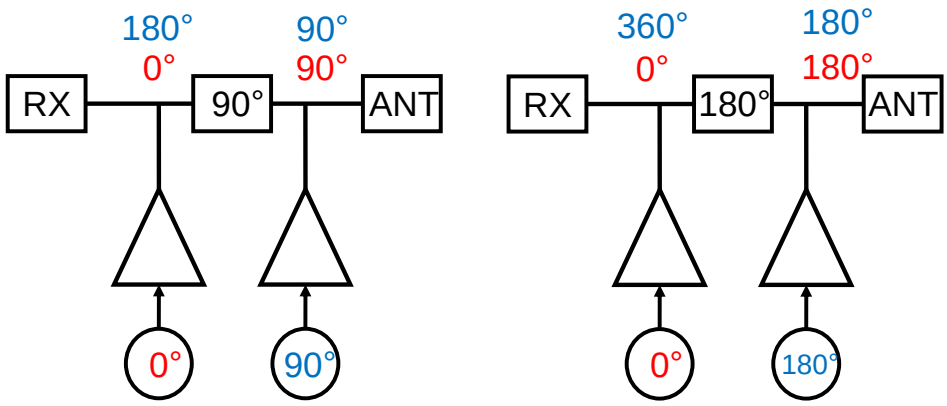


Figure 5.2: The two tap case. Left subpanel (at f_{op}) depicts the ideal scenario: all the signal input adds constructively at the ANT port, and nulls at the RX port. The right subpanel (at $2f_{op}$) is the worst case scenario, isolation cannot be achieved no matter what the inputs are.

which then tap into either side of a delay line. On one end of the delay line is the receiver, and the other side is the RF/antenna port. Assume that for a particular operating frequency f_{op}, the phase delay of the line is 90 degrees, and the receiver and RF ports are impedance matched. Let us also assume that the sub-transmitter outputs (R_{out}) are high impedance. Then, if the sub-transmitter on the left has a phase shift of 0 degrees, and the right sub-transmitter has a phase shift of 90 degrees (for simplicity, we assume that the input signals are of the same magnitude), then the signals add up coherently at the RF port, and destructively at the RX, providing perfect isolation. In this scenario all of the signal power injected into the line adds up at the RF port, and the TX signal is completely nulled at the receiver. As the frequency of operation f_{op} is increased, the fixed time delay translates to a greater phase shift for the signal. At $2f_{op}$, the phase delay is now 180 degrees. Now, there is no combination of input angles that will result in a scenario like the 90 degree case since the phase difference between the two superposed signals is equal in both directions. No matter what angles/gains we choose in this case isolation is not possible. We

can show this simply by looking at the matrix that relates the input currents to the voltages. If we define the input currents as a vector $i = \left[\begin{smallmatrix} i_1 \\ i_2 \end{smallmatrix}\right]$, and the output voltages as a vector $v = \left[\begin{smallmatrix} v_1 \\ v_2 \end{smallmatrix}\right]$. we can use a 2×2 impedance matrix Z to relate them to one another such that $v = Zi$. Note that in this case $\left[\begin{smallmatrix} v_1 \\ v_2 \end{smallmatrix}\right] = \left[\begin{smallmatrix} v_{RX} \\ v_{ANT} \end{smallmatrix}\right]$, and our goal is to have the input signal add up coherently for v_{ANT} and null for v_{RX}. For the left case of Fig. 5.2, we have:

$$Z(f_{op}) = Z_0 \begin{bmatrix} 1 & e^{j90} \\ e^{j90} & 1 \end{bmatrix} = Z_0 \begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} \tag{5.1}$$

while for the right case we have:

$$Z(2f_{op}) = Z_0 \begin{bmatrix} 1 & e^{j180} \\ e^{j180} & 1 \end{bmatrix} = Z_0 \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{5.2}$$

Now, it's important to note that to null the signal at the RX port the current vector $i = \left[\begin{smallmatrix} i_1 \\ i_2 \end{smallmatrix}\right]$ must be orthogonal to the first row of the impedance matrix. Then, the multiplication of the second row of Z with the input current vector determines the output voltage at the antenna port. So, for Fig. 5.2 example we can see that the current $i = \left[\begin{smallmatrix} 1 \\ e^{j90} \end{smallmatrix}\right]$ is orthogonal to the top row of $Z(f_{op})$ but not the top row of $Z(2f_{op})$. Also note that the determinant of $Z(2f_{op})$ is zero, which is why $Z(2f_{op})$ is not invertible and there is no solution set that satisfies our constraints. However, invertibility is not the only measure of physical realizability or efficiency of this system. In this context, the conditioning of the impedance matrix Z is very important for feasibility of implementation. From this simple two-tap example we can see that for a fixed time delay either isolation or efficiency degrades as frequency changes, and for some frequency combinations there are no inputs that can achieve isolation.

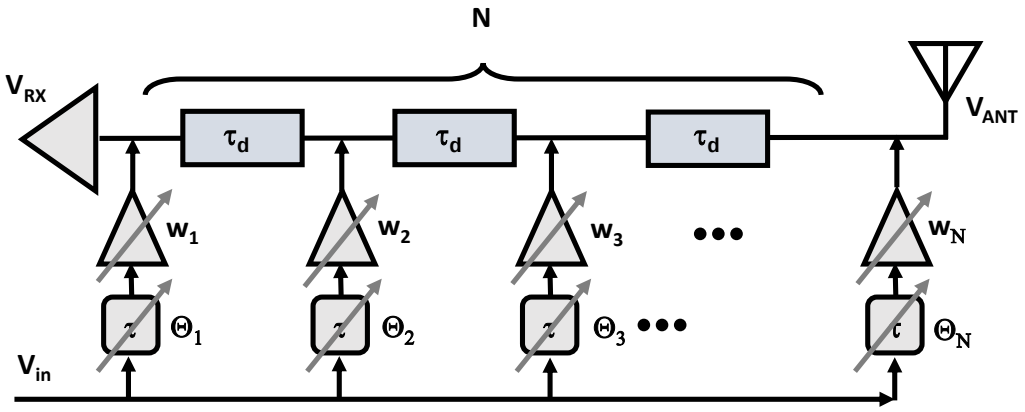


Figure 5.3: Distributed transmission line based amplifier. The N subtransmitters are separated by time delays τ_d. The inputs have a complex weights w_i with phase rotation Θ_i. The input is shared between the subtransmitters, and while one end of the line is terminated by the receiver, the other end is terminated by the ANT port.

Ensuring isolation throughout different frequencies while preserving reasonable levels of output power and efficiency require more degrees of freedom than two. The simplest answer to provide the additional degrees of freedom in this system is to increase the number of stages.

5.2.2 Analysis as a Distributed Amplifier

As a known multi-tap structure, consider the classic distributed amplifier as shown in Fig. 5.3, as in [66]. In this case, N subtransmitters are separated by time delays τ_d. Then, the inputs are phase shifted relative to each other by Θ_i, such that the TX baseband signal V_{in} adds constructively on the antenna port (i.e. that is $\vec{w}$ is antiparallel to bottom row of the Z matrix). There is some intrinsic cancellation achieved at the RX port (see Fig. 5.4), albeit not adequate for duplex applications since it is around 15dB [14]. Furthermore, at frequency extremes of 0Hz, and $1/2\tau_d$, the intrinsic cancellation fails. Note that adding

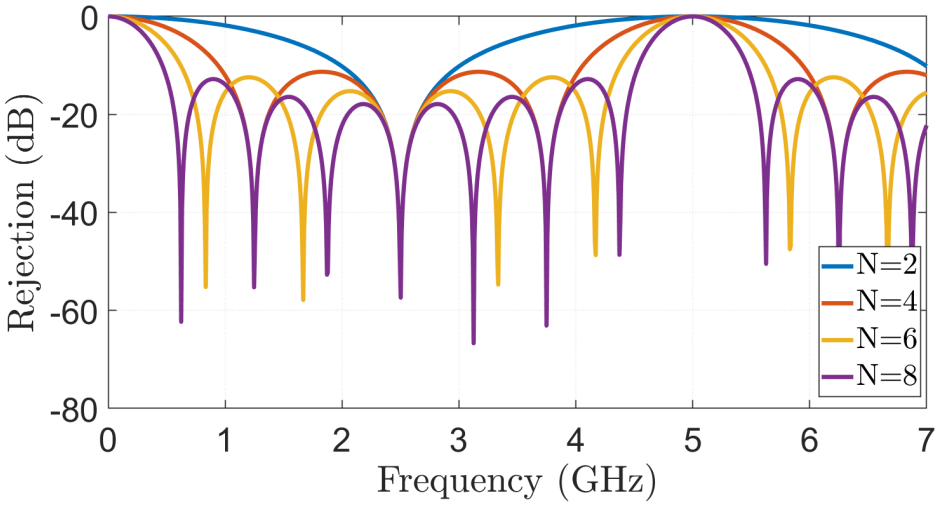


Figure 5.4: Intrinsic cancellation of a distributed amplifier for different number of stages: N=2,4,6,8. $\tau_d = 100ps$.

additional stages improves magnitude and frequency range of cancellation mid-band.

To achieve isolation across frequency, we allow independent control of w_i's such that we can null the signal at the RX port as well. The optimal tap vector w_i can be computed by observing the two ends of the transmission line V_{ANT} and V_{RX}:

$$\frac{V_{ANT}}{V_{in}} = \sum_{k=0}^{N-1} w_k e^{j\omega_{TX}\tau_d k} = \overrightarrow{h_1(\omega_{TX})} \cdot \vec{w} \tag{5.3}$$

$$\frac{V_{RX}}{V_{in}} = \sum_{k=0}^{N-1} w_k e^{j\omega_{TX}\tau_d (N-1-k)} = \overrightarrow{h_2(\omega_{TX})} \cdot \vec{w} \tag{5.4}$$

where V_{ANT},V_{RX},V_{in} are the voltages at the respective terminals, and w_i are the complex input gain values.

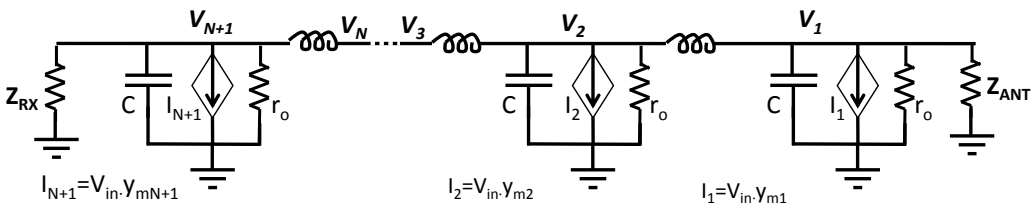


Figure 5.5: Linear system figure with R, L and C. The subtransmitters are modeled as current sources.

5.2.3 Linear RLC Model

While the time-delay model described in the previous section is a useful start, implementing for single GHz frequencies on chip is not feasible due to the large length of the delay lines needed. Now, we introduce a more realistic circuit model where discrete components are used to create a lumped model as shown in Fig. 5.5. The artificial transmission line is constructed by LC T-sections composed of series L and shunt C's. The inductors have a finite Q which can be modeled as a series resistance:

$$R_s = \frac{\omega L}{Q} \tag{5.5}$$

Each end of the line is terminated by the Z_{RX} and Z_{ANT}, and the subtransmitters are modeled as current sources with a shunt $R_{out} = r_o$ and C. Kirchhoff's Current Law equations below at each node of an N-stage T-line describes how I_i relates V_i as follows for different nodes:

$$\begin{aligned} &\text{Node i} = 1: \\ &0 = I_1 + V_1(j\omega C + \frac{1}{r_o} + \frac{1}{Z_{ANT}}) + \frac{V_1 - V_2}{\omega L(j + \frac{1}{Q})} \end{aligned} \tag{5.6}$$

$$\begin{aligned}&\text{Nodes } 1 < \text{i} < \text{N} + 1 : \\ &0 = I_i + V_i(j\omega C + \frac{1}{r_o}) + \frac{2V_i - V_{i-1} - V_{i+1}}{\omega L(j + \frac{1}{Q})}\end{aligned} \tag{5.7}$$

$$\begin{aligned}&\text{Node i} = \text{N} + 1 : \\ &0 = I_{N+1} + V_{N+1}(j\omega C + \frac{1}{r_o} + \frac{1}{Z_{RX}}) + \frac{V_{N+1} - V_N}{\omega L(j + \frac{1}{Q})}\end{aligned} \tag{5.8}$$

Therefore, we can summarize the relationship between I_i and V_i as an admittance matrix Y:

$$Y = \begin{bmatrix} y_{11} & y_{12} & 0 & \cdots & 0 & 0 \\ y_{21} & y_{22} & y_{23} & \cdots & 0 & 0 \\ 0 & y_{32} & y_{33} & \cdots & 0 & 0 \\ 0 & 0 & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & y_{N-1,N-2} & y_{N-1,N-1} & y_{N-1,N} \\ 0 & 0 & 0 & 0 & y_{N,N-1} & y_{N,N} \end{bmatrix}$$

where:

$$y_{i,i} = j\omega C + \frac{1}{r_o} + \frac{2}{\omega L(j + \frac{1}{Q})} \tag{5.9}$$

$$y_{i,i-1} = y_{i-1,i} = \frac{1}{\omega L(j + \frac{1}{Q})} \tag{5.10}$$

$$y_{1,1} = j\omega C + \frac{1}{r_o} + \frac{1}{Z_{RX}} + \frac{1}{\omega L(j + \frac{1}{Q})} \tag{5.11}$$

$$y_{N,N} = j\omega C + \frac{1}{r_o} + \frac{1}{Z_{ANT}} + \frac{1}{\omega L(j + \frac{1}{Q})} \tag{5.12}$$

$$Z = [Y^{-1}] \tag{5.13}$$

While the RLC structure shown in 5.5 is functional, it suffers from limited bandwidth. We can add extra LC stages as shown in Fig. 5.6 without loss of generality (i.e. without any explicit change in terms of the Y matrix).

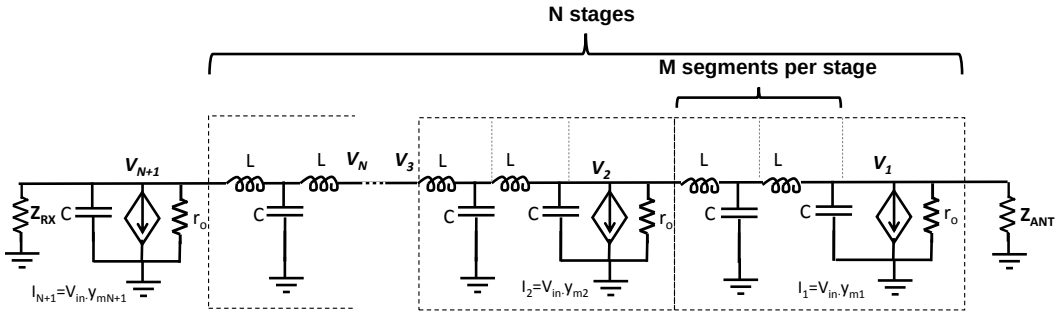


Figure 5.6: Linear system figure with R, L and C. Extra delay stages are added to increase the total time delay of the transmission line to broaden the range in which the TL can operate.

5.3 Calculating Ideal Weights

Now that we have created an RLC model for the artifical lumped transmission line based amplifier and summarized the relationship between the inputs $\vec{i}$ and outputs $\vec{v}$, we can describe the constraints and goals of the system. Our goal is to **1.** maximize power out at the antenna P_{out}, **2.** minimize TX power reaching the RX port P_{RX}, and **3.** achieve (1) and (2) as efficiently as possible. We can transform the first two goals from power to voltage to fit our system description

by considering the impedance at the two nodes: Z_{ANT} and Z_{RX}. Then, for a particular output power level P_{out}, the voltage at the antenna port is V_{out}, and we want to minimize the TX voltage at RX such that $V_{RX} = 0$.

$$\begin{bmatrix} V_{out} \\ 0 \end{bmatrix} = \begin{bmatrix} V_{ANT} \\ V_{RX} \end{bmatrix} \tag{5.14}$$

We can reframe this optimization problem to only include two rows of the impedance matrix Z since the internal voltages are "free" variables.

$$\begin{bmatrix} V_{out} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \vec{v} = - \begin{bmatrix} 1 & \cdots & 0 \\ 0 & \cdots & 1 \end{bmatrix} Z\vec{i} \tag{5.15}$$

$$X = - \begin{bmatrix} 1 & \cdots & 0 \\ 0 & \cdots & 1 \end{bmatrix} Z, \begin{bmatrix} V_{out} \\ 0 \end{bmatrix} = X\vec{i} \tag{5.16}$$

Now, since X is not square, it cannot be simply inverted. Since this system is underdetermined, we use the right pseudoinverse to find the solution for $\vec{i}$.

$$\vec{i} = X^*(XX^*)^{-1} \begin{bmatrix} V_{out} \\ 0 \end{bmatrix} = X^\dagger \begin{bmatrix} V_{out} \\ 0 \end{bmatrix} \tag{5.17}$$

It is important to note that the pseudoinverse $X^\dagger$ is the L2-norm minimizer of $\vec{i}$. $\|i\|_2$ to a first order (as we will explain in Section IV) is a measure of efficiency in the system.

5.4 Impact of Circuit Imperfections

5.4.1 Effect of Number of Stages on Efficiency

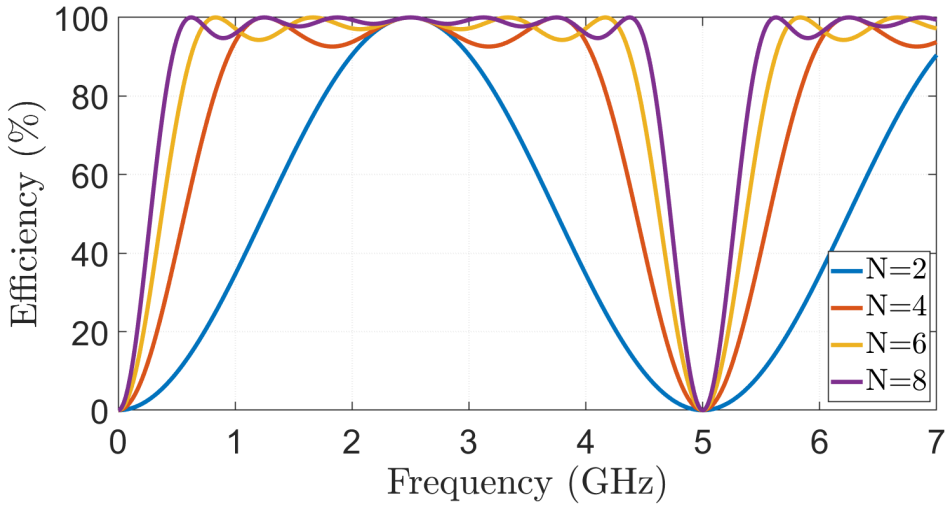


Figure 5.7: Percentage efficiency for a distributed amplifier for different number of stages: N=2,4,6,8. $\tau_d = 100ps$.

Efficiency degrades between these two frequency extremes, as shown in Fig. 5.7. System efficiency improves as the number of subtransmitters increase.

5.4.2 Impact of Finite Q and R_{out} TX Efficiency and RX Loss

The inductor quality factor is the most important figure that determines the insertion loss of the transmission line. Especially at high frequencies, the inductor Q factor starts to impact the RX S_{21}. Fig. 5.8 shows the effects of different Q factors on insertion loss.

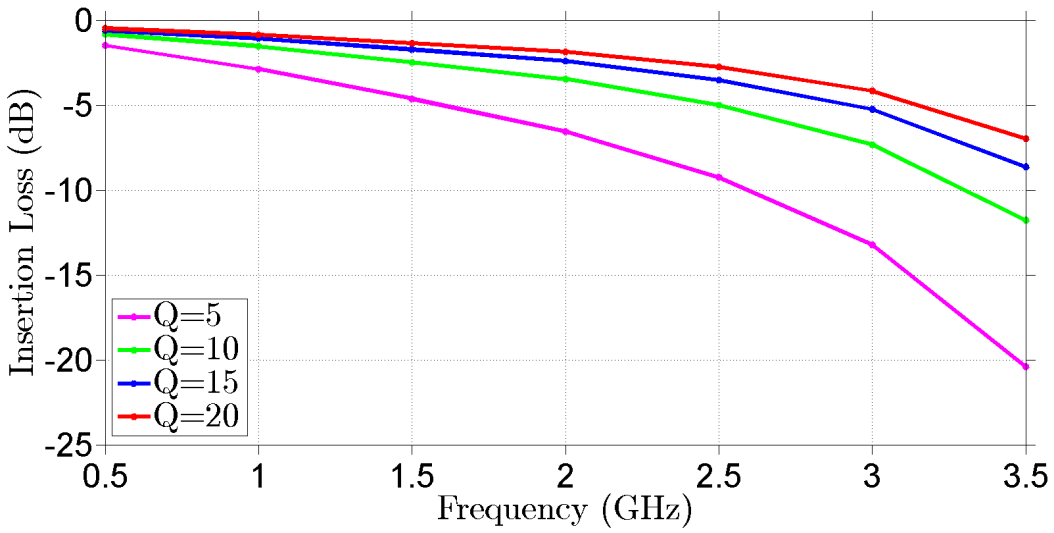


Figure 5.8: Effect of inductor Q factor on RX insertion loss. N=6, 7-bit precision.

5.4.3 Effects of Complex Weight Quantization

To see how the quantization of magnitude and phase for each PA affects isolation, we define M and N as the ENOB of resolution for magnitude and phase respectively. Therefore, the maximum error in a single PA's magnitude is $\frac{A_{max}}{2^{M+1}}$ and the maximum phase error is $\frac{2\pi}{2^{N+1}}$. Considering these errors in each sub-transmitter's output, we can then find an upper bound on the degradation of TX output power and TX-RX isolation.

To find this bound, we start by modeling the n^{th} sub-transmitter output with quantization errors as a voltage phasor ($\vec{V}_{TX,n}$) equal to the sum of the ideal, desired phasor ($\vec{V}_{TX,n,ideal}$) plus an error due to magnitude quantization ($\Delta\vec{m}$), and an error due to phase quantization ($\Delta\vec{\phi}$). Assuming $\Delta\vec{\phi}$ is small, we can see that $\Delta\vec{\phi} \perp \vec{V}_{TX,n,ideal}$, while $\Delta\vec{m} \parallel \vec{V}_{TX,n,ideal}$. If we choose the phase of $\vec{V}_{TX,n,ideal}$ to be 0° and $A_{max} = 1$ for simplicity, we get

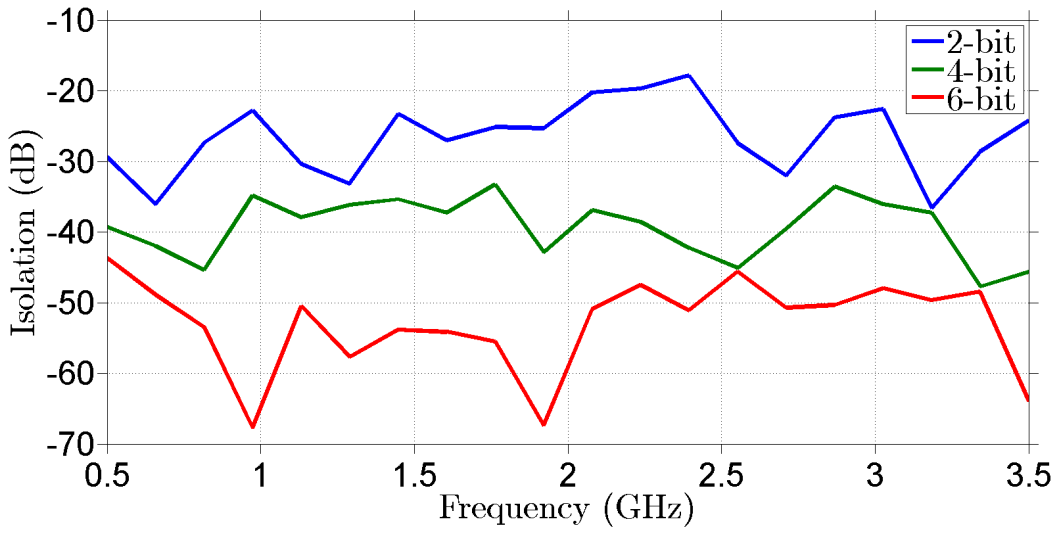


Figure 5.9: Isolation as a function of different input weight bit precision. The pseudoinverse algorithm is used. N=6.

$$\Delta\vec{m} = \frac{\pm 1}{2^{M+1}} \quad \text{and} \quad \Delta\vec{\phi} = \pm A_n j \tan[\frac{2\pi}{2^{N+1}}] \qquad M \geq 1, N \geq 3 \tag{5.18}$$

where the constraints on M and N are sufficient to satisfy the assumption that $\Delta\vec{\phi}$ is small. For the purposes of finding an upper limit on the effect of quantization errors, we can see that assuming $A_n = A_{max} = 1$ gives the largest possible magnitude for $\Delta\vec{\phi}$. So, applying the small angle approximation for tangent we can bound the total magnitude of error for a single sub-transmitter:

$$|\Delta\vec{m} + \Delta\vec{\phi}| \leq \sqrt{2^{-2(M+1)} + 4\pi^2 \cdot 2^{-2(N+1)}} \tag{5.19}$$

To write a lower bound on the total transmit signal $\vec{V}_{TX}$, we can consider the worst-case scenario for all N_{st} error vectors—The case where each of the N_{st} error vectors align perfectly and in the opposite direction to $\vec{V}_{TX}$. In that case,

$$|\vec{V}_{TX}| \geq |\vec{V}_{TX,ideal}| - N_{st} \cdot |\Delta\vec{m} + \Delta\vec{\phi}| \tag{5.20}$$

where $|\vec{V}_{TX,ideal}| \in [0, N_{st}]$ depending on how well each sub-transmitter's signal adds in phase at the TX port. Assuming our ideal sub-transmitter weights give perfect cancellation at the RX, we can see that an error vector at the TX port will propagate down the lossless transmission line and will appear at the RX port with the same magnitude. Therefore, $|\vec{V}_{RX}| = N_{st} \cdot |\Delta\vec{m} + \Delta\vec{\phi}|$, and

$$\text{Isolation} \geq \frac{|\vec{V}_{TX,ideal}|}{N_{st} \cdot |\Delta\vec{m} + \Delta\vec{\phi}|} - 1 \tag{5.21}$$

5.4.4 Finite Frequency Errors: Cancellation Bandwidth

It is critical to note that the impedance matrix Z that relates inputs $\vec{i}$ to outputs $\vec{v}$ is a function of frequency. We compute the input weights $\vec{i}$ such that we null

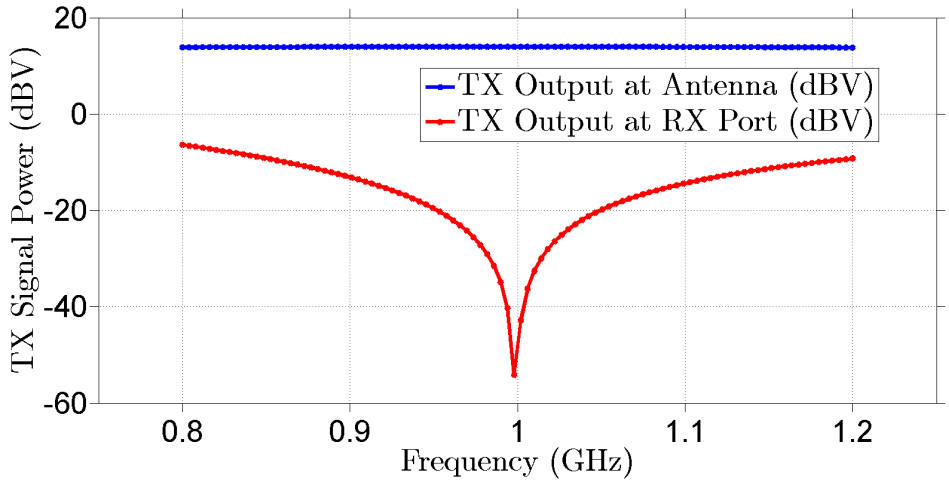


Figure 5.10: Isolation as a function of frequency. Cancellation weights have been chosen for a center frequency of 1GHz. Note that isolation is around 55dB at the RX port.

the transmit signal at the RX port at the TX frequency f_{TX}. However, as we step away f from f_{TX}, $Z(f)$ starts to change and cancellation starts to degrade. It is important to note that the TX power within this frequency range does not degrade significantly. While the cancellation notch at the frequency (f_{TX}) at which we computed the weights is deep (∼55dB, for $N = 6$ and a 7-bit resolution as shown in Fig. 5.10), > 15dB of cancellation is achieved at frequencies that are 200MHz away from the center frequency for a center frequency of 1GHz. This has important noise implications that will be discussed in Section VII.

We use the term cancellation bandwidth to refer to the bandwidth of the distributed duplexing cancellation method. It is important to note that this is separate from the placement of the notch, which depends on the frequency of operation and tunable over octaves as shown in [64].

5.4.5 Changes in Termination Impedance

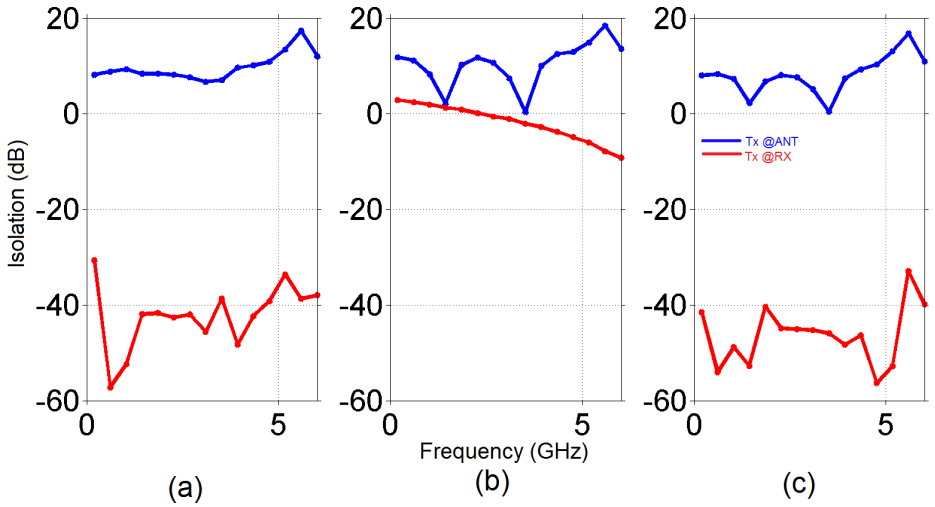


Figure 5.11: Effects of changing the antenna port impedance for isolation, initial(left), uncalibrated (middle), calibrated (right).

Many duplexers' isolation is highly sensitive to antenna port impedance.

When subjected to a 1:2 impedance mismatch to a 50Ω line without adaptation, the isolation and output power both suffer. The left subpanel of Figure 5.11 is the initial state of the transceiver where the antenna impedance is matched to the TL. Whereas the middle subpanel shows the degradation in both TX power and isolation when the antenna impedance is doubled while the weights are kept the same. The right panel shows the adaptation of weights to the new impedance, and shows that the system is able to recover back to the previous output power level and isolation.

5.5 Frequency Selective Degeneration

A duplexer not only has to prevent large transmitted signals from saturating or destroying the receiver but also needs to help suppress TX noise at RX band. Both add noise and shunting loss contributes to RX noise figure (NF), and so must be suppressed to keep RX NF at acceptable levels. In this section, we discuss the theory of N-path based frequency selective degeneration to help suppress TX-generated noise in the RX while still preserving TX in-band gain.

5.5.1 TX-induced RX Noise and Loss

A common source (CS) based PA will generate an output noise of

$$\overline{v_{txPA}^2} = 4kT\gamma G_m {R_L}^2 \tag{5.22}$$

where G_m is the composite transconductance of the PA and R_L is the load of the PA. In addition, any noise on its input (based on pre-amplifiers, mixers, TX

phase noise) will be amplified by the PA gain, $A_v = G_m R_L$. Note that this applies even to switched PAs, since phase noise (and equivalent pre-amp noise) passes through. Additionally, the output impedance of the PA will shunt the incoming RX signal by a factor relating to $Z_{out,PA}$, directly impacting RX noise figure. If the amplifier is degenerated by an impedance Z_{deg}, this directly impacts noise such that

$$G_{m,deg} = \frac{g_m}{1 + g_m Z_{deg}} \tag{5.23}$$

and therefore

$$\overline{v^2_{txPA,deg}} = 4kT\gamma G_{m,deg} {R_L}^2 \tag{5.24}$$

However, if the impedance Z_{deg} can be designed to to be high at f_{RX} but low at f_{TX}, then loss and noise at f_{RX} can be suppressed without degrading gain at f_{TX}.

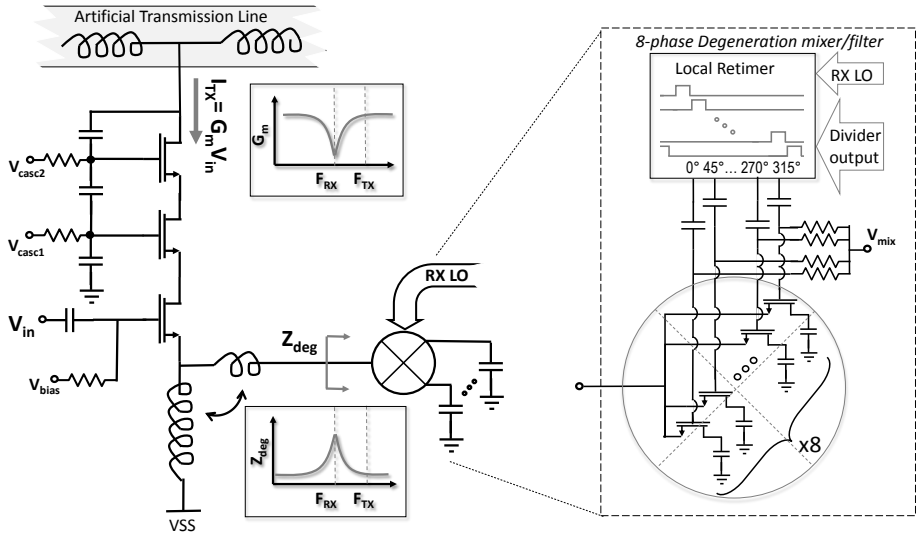


Figure 5.12: Frequency selective degeneration. An N-phase passive mixer is attached to the source of the input device. The mixer runs on the RX LO, degenerating the PA in the RX band.

5.5.2 Passive Mixer Impedance Properties

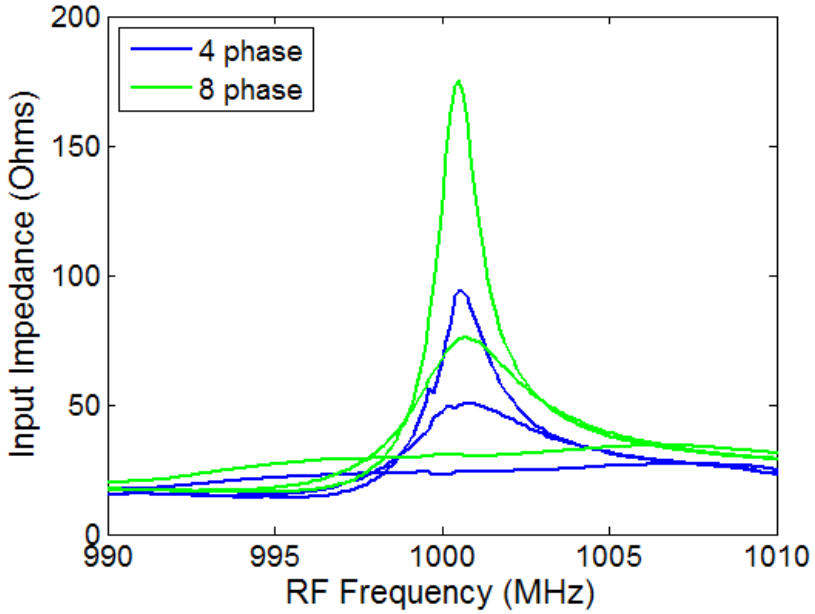


Figure 5.13: Passive mixer input impedance for 4 and 8 phase mixers. Note the difference between out of band and in band impedances.

Previous work [60] has shown that a passive mixer driven by N non-overlapping, phase-split LO pulses and loaded with baseband capacitors C_L has an impedance of

$$Z_{in} = R_{sw} + \frac{R_{sh}\gamma Z_B}{R_{sh} + \gamma Z_B} \tag{5.25}$$

where $Z_B = \frac{1}{j(\omega_{RF}-\omega_{LO})C_L}$ and $\gamma = \frac{1}{N}sinc^2(\frac{\pi}{N})$. R_{sw} is the resistance of the mixer switches and the R_{sh} is the virtual shunt resistance due to harmonic loss effects. R_{sh} is due to the re-radiation loss on the source impedance, and is bounded by:

$$\begin{aligned} R_{sw}\frac{sinc^2(\pi/N)}{1-sinc^2(\pi/N)} &\leq R_{sh} \\ &\leq (R_{sw}+R_s)\frac{sinc^2(\pi/N)}{1-sinc^2(\pi/N)} \end{aligned} \tag{5.26}$$

where R_s is the source resistance at the RF port. The value of R_{sh} decreases from its upper bound towards its lower bound as the frequency increases.

5.5.3 Circuit Diagram

Equation 5.25 implies that $Z_{in} \approx R_{sw}$ if $\omega_{RF} >> \omega_{LO}$, i.e. if the RF frequency is out of band. For in band frequencies $Z_{in} \approx R_{sh}$. We leverage this impedance relation by attaching the RF port of an N phase passive mixer to the source terminal of the input device of a common source based PA. DC bias current must be brought separately by a choke inductor [64] (or omitted by a complimentary design). Away from the N-path filter's LO frequency, the amplifier is in the high-gain, non-degenerated regime (i.e. TX band) the PA transconductance is:

$$G_m(\omega_{TX}) = \frac{g_{mPA}}{1 + g_{mPA}R_{sw}} \tag{5.27}$$

Conversely, close to the N-path filter's LO frequency, in the low-gain, degenerated regime, the G_m is reduced:

$$G_m(\omega_{TX}) = \frac{g_{mPA}}{1 + g_{mPA}R_{sw}} \frac{1}{A_{deg}} \tag{5.28}$$

where $A_{deg} = \frac{1}{1-N\gamma} = \frac{1}{1-sinc^2(\pi/N)}$. This implies that the gain in the RX band (in-band) relative to the TX band (out-of-band) will be attenuated by A_{deg}. In the $N = 4$ phase case, $A_{deg} = 5.3(14.4\text{dB})$, and in the $N = 8$ phase case, $A_{deg} = 19.9\,(25.9\text{dB})$. Furthermore, the degeneration technique not only reduces the TX gain in the RX band, it also boosts the transmitter output impedance to reduce shunting of the RX signal. Specifically, while the output impedance of the PA at the TX band is $Z_{out}(\omega_{TX} = Z_{out,PA}(1 + g_{mPA}R_{sw})$ at the RX band is boosted by A_{deg} such that $Z_{out}(\omega_{RX} = Z_{out,PA}(1 + g_{mPA}R_{sw})A_{deg}$.

5.6 General Noise Contributors to the Duplexing Transceiver

The noise requirements on the TX signal from a dBc perspective are very stringent if minimal RX NF degradation is required. For example, if the output power is +24dBm, and only 3dB of NF degradation is desired, this implies a -198dBc relative noise floor at the RX band. Clearly, significant care must be taken to suppress this noise. Furthermore, a number of different noise mechanisms can contribute to the TX output noise in the RX band: **1.** baseband input (including DAC quantization noise): n_{txin} **2.** sub-transmitter baseband circuitry, n_{txbb} **3.** sub-transmitter RF circuitry, such as the RF pre-amplifier and the upconversion mixer, n_{txRF}, **4.** the noise due to the power amplifier, n_{txPA} **5.** the TX LO noise due to shared circuitry, $n_{txLOmain}$ **6.** the TX LO noise due to local buffer circuitry, $n_{txLOlocal}$ **7.** the RX LO noise due to shared circuitry, $n_{rxLOmain}$ **8.** the RX LO noise due to local buffer circuitry, $n_{rxLOlocal}$. The different noise sources are shown in Fig. 5.14 below.

Three mechanisms can act to suppress such noise sources, however. The first mechanism is simply the low-pass nature of the TX baseband, thus noise sources n_{txin} and n_{txbb}, the baseband noise of each sub-transmitter along with any shared

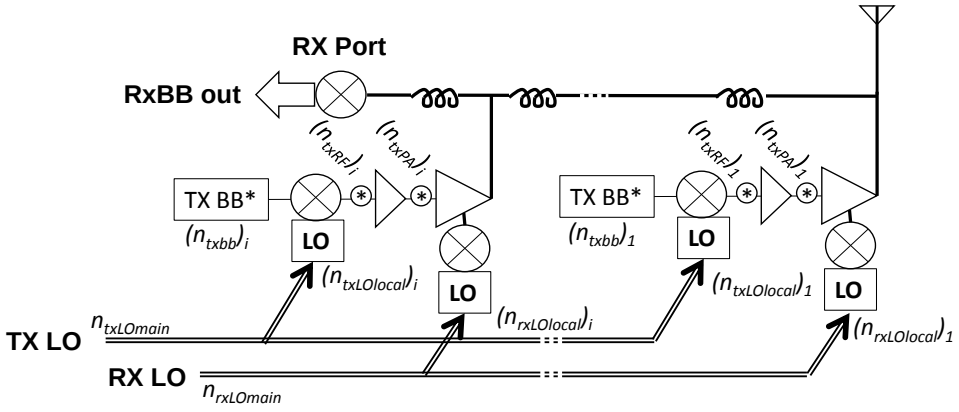


Figure 5.14: Different noise contributors.

baseband noise, will be suppressed by at least one low-pass pole. The second mechanism is through the frequency selective degeneration, which suppresses RX-band noise from mechanisms (1-5), including baseband and RF mechanisms (PA), but also acts to suppress TX LO phase noise. However, as discussed below, this degeneration also provides the primary path for the generation of TX noise affecting the RX: $n_{rxLOmain}$, $n_{rxLOlocal}$. The third noise suppression mechanism is a side effect of the suppression of the TX signal itself in the distributed duplexing: any noise that is correlated across subtransmitters is subject to the same suppression method as the TX signal itself. Provided that the RX frequency is not too distant from the TX frequency, much of the suppression still will be active within the degeneration bandwidth. This mechanism applies to correlated noises, n_{txin}, $n_{txLOmain}$, and $n_{rxLOmain}$, as discussed in more detail in the next section. These effects are summarized in Table 5.1.

The need for high TX output power, combined with a low output impedance presented by the RF TL (25Ω for a system directly matched to 50Ω) sets the individual PA transconductance G_m(ω_{TX}, scaled by number of subtransmitters N. However, this G_m also sets the uncorrelated noise contributions from the PAs, which is fundamental given a certain output impedance, power level and input voltage swing. While increasing the input swing will help with this problem, it typically implies some gain in the preceding stages, increasing the noise contribution of these stages. Also, most often passive mixers have limited swing ranges. Frequency selective degeneration can mitigate this problem by suppressing uncorrelated noise from the PAs and preceding stages.

Table 5.1: Different Methods of Noise Suppression

Noise Source	**Helped by Filtering?**	**Helped by Degeneration?**	**Helped by Distributed Cancellation?**
n_{txin}	Yes	Yes (by A_{deg}^2)	Yes
n_{txbb}	Yes	Yes (by A_{deg}^2)	No
n_{txRF}	No	Yes (by A_{deg}^2)	No
n_{txPA}	No	Yes (by A_{deg})	No
$n_{txLOmain}$	No	Yes (by A_{deg}^2)	Yes
$n_{txLOlocal}$	No	Yes (by A_{deg}^2)	No
$n_{rxLOmain}$	No	No	**Yes**
$n_{rxLOlocal}$	No	No	No

5.7 Impacts of Distributed Duplexing on Noise

As with any transceiver, receiver noise figure (NF) is a critical system parameter. Because distributed transmitters connect N PA's to the receiver input, any noise produced by the transmit circuitry at the receive frequency directly couples into the receiver, degrading its NF. Therefore, all TX noise mechanisms must be suppressed and/or minimized at the RX frequency. In Table 5.1, we summarize the various noise sources (both from RX and TX) and what, if any mechanisms suppress this noise at the RX frequency.

5.7.1 Noise Suppressed by Frequency-Selective Degeneration

The main mechanism by which we suppress noise at the RX frequency is by degenerating each PA at the RX frequency with the frequency selective degeneration mechanism explained in Section V. This reduces the gain of each PA at

the RX frequency, meaning the drain noise of the PA itself, any noise from the baseband TX circuitry, and TX LO phase noise added during upconversion is suppressed. The amount of suppression depends on the effectiveness of the degeneration circuitry in reducing the PA's gain around the RX frequency. In [64] we demonstrated a 15dB decrease in PA gain (and therefore TX noise) at the RX frequency using 8-phase N-path filters.

5.7.2 Noise Unaffected by Degeneration

The primary noise mechanism unaffected by degeneration is phase noise on the RX LO, which is added to TX signals in the degeneration mixers. Luckily, oscillator phase noise at small offset frequencies that follows a $1/f^2$ response is canceled in N-path filters according to [67]. Therefore, the critical specification for the RX LO is the white noise floor seen at large offsets, which is generally lower than close in phase noise.

Although the partial noise suppression inherent to N-path filters reduces the noise contribution of RX LO phase noise, any un-suppressed white phase noise will directly degrade RX NF. Assuming in-band noise power at the receiver input must be below a certain threshold n_{max}, we can calculate the maximum allowable white phase noise floor for the RX LO (n_{RXLO}). Considering only RX LO phase noise, the noise current at the source of each PA will have power $n_{RXLO} \cdot P_{TX}$ where P_{TX} is the TX signal power. Because we are considering white phase noise, the current noise at each PA's source is uncorrelated with every other PA's current noise, and each PA's contribution will RMS sum at the RX input:

$$n_{RX} = \sqrt{N_{st}} \cdot (P_{TX} \cdot n_{RXLO}) \leq n_{max} \tag{5.29}$$

Solving for n_{RXLO} gives:

$$n_{RXLO} \leq n_{max} \div (\sqrt{N_{st}} \cdot P_{TX}) \tag{5.30}$$

So, as per-subtransmitter TX power rises, the white noise floor of the RX LO must fall if the same maximum noise power at the RX is not to be exceeded. This means that far-out phase noise in the RX LO is critical to the noise performance of the RX whenever a significant TX signal is being generated.

5.8 Conclusion

We have presented the design framework for a distributed duplexing transceiver and analyzed its theoretical bounds for figures of merit such as isolation, and efficiency. We analyzed the effects of nonidealities such as finite frequency deviations and quantization of input weights on different system figures of merit. Future work includes open questions on how to expand the bandwidth range of distributed cancellation and elimination uncorrelated RX LO phase noise due to the degeneration mixer on the RX NF.

CHAPTER 6

FD CAPABLE WIDELY TUNABLE TRANSCEIVER

6.1 Introduction

Truly flexible, integrated RF front ends will need to support a variety of duplex scenarios including TDD, FDD, and likely single channel full duplex (FD). The front end must function over a range of RX/TX frequencies and spacings, while meeting spectral mask requirements and suppressing TX signals, distortion, harmonics, and noise at the RX port. Same channel FD is particularly challenging due to self-interference (SI), requiring SI cancellation across the RF, analog and digital domains [68]. Ideally, this is accomplished without costly off-chip filters, diplexers or circulators, and also using a single antenna interface such as in [7] or [69].

In this Chapter, we present a dual technology duplexing front-end, similar to what we presented in Chapter 4, that supports TDD, FDD, and FD while implementing predistortion to suppress spurious TX emissions, and spurious emissions at harmonics of the TX frequency. The design combines a programmable complex-weighted distributed transmitter whose subtransmitters tap into an LC based transmission line. A non-reciprocal distributed PA degeneration network suppresses signal and noise of individual transmitters at the receiver, including when RX and TX are closely spaced or identical.

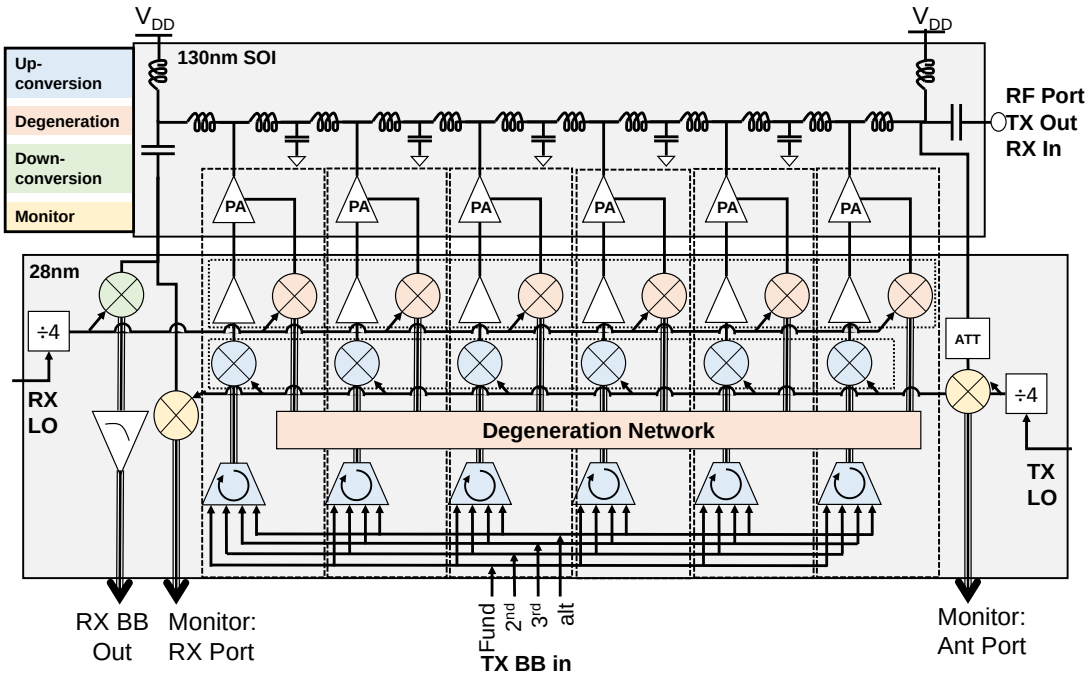


Figure 6.1: System block diagram.

6.2 System Discussion

Fig. 6.1 shows the block diagram of our distributed duplexer. As in [64], the previous transceiver introduced in Chapter 4, complex weighting of baseband TX signals before upconversion provides suppression at the RX while maximizing signal at the antenna port. In FDD mode transmitter noise is suppressed at the receiver frequency with frequency-selective degeneration. Compared to the earlier generation transceiver, this system offers a number of improvements. First, we take advantage of the speed and compactness of 28nm CMOS for LO and mixer circuits while implementing the high output voltage PAs and high-Q passives of the transmission line in an SOI process, splitting the design between two chips. The SOI process offers low substrate loss, therefore reducing the loss of the transmission line inductors. A new mode of operation, FD mode, is enabled by the distributed degeneration network. Low distortion transmission is

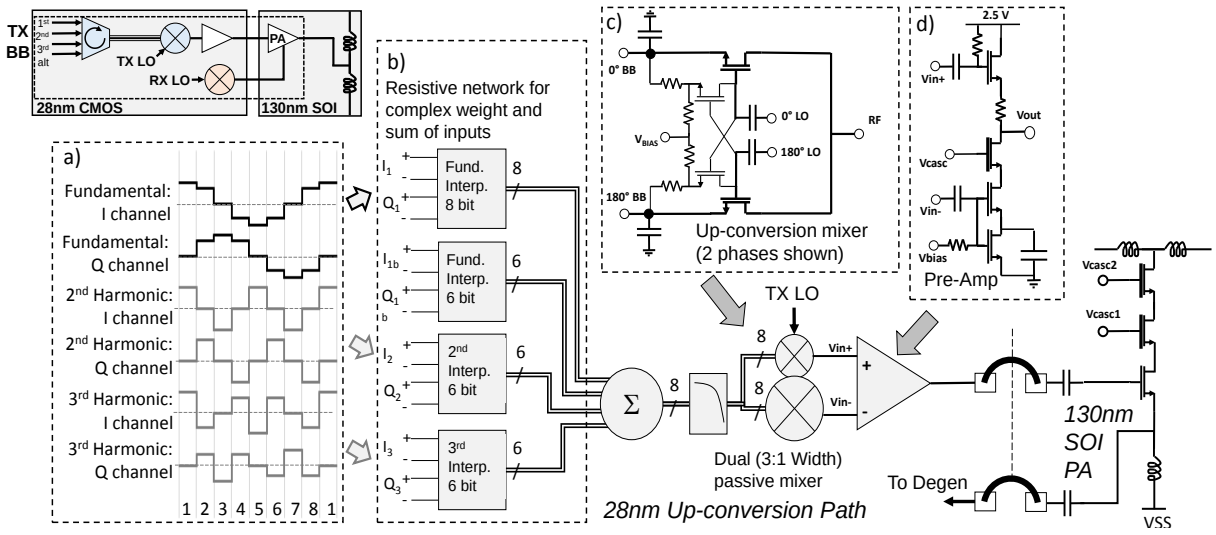


Figure 6.2: The upconversion chain.

enabled by the addition of harmonic suppression both for spectral mask compliance and to avoid saturating the RX. The architecture employs 15 8-phase passive mixers with associated circuitry, driven by two LO chains (RX and TX) to implement the following capabilities:

6.2.1 Mixer Dynamic Range Improvements

Proper operation of frequency-selective degeneration requires that degeneration mixers support the large RF signal swings that may be present due to the TX signal. As swing on the RF port becomes large, it may drive the source terminals to low enough voltage to turn mixer transistors on even when their gates are "off", degrading performance. To mitigate this effect, the LO pulse generators driving mixer gates were designed to drive the gates below the DC voltages of the RF and baseband ports while still driving the mixers' gates to their maximum allowable voltage when on.

A similar problem exists in the upconversion mixers, where it is desirable

to maximize SNR in individual TX chains by maintaining strong TX signals. To further improve in-band swing in the upconversion mixer, the gates were DC coupled through a 2:1 resistive voltage divider to their respective baseband terminals, such that the gates partially track the baseband inputs, increasing signal handling by about 50% (Fig. 6.2c, [70]). Additionally, to minimize noise added by the PA pre-amp, an asymmetric, anti-phase pair of upconversion mixers were used to drive a push-pull PA driver (Fig. 6.2d).

6.2.2 Harmonic Predistortion

As shown in Fig. 6.2b, four resistive interpolation blocks were implemented in each TX upconversion chain. The first of these enables individual magnitude and phase control for each upconversion chain. The second is a similarly configured network that allows for injection of an additional baseband signal to perform in-band predistortion with a distinct distribution of amplitude and phase. The remaining two exploit harmonic conversion modes of the 8-phase upconversion mixer to inject second and third harmonic predistortion terms to cancel harmonics generated by the nonlinearity in the PA's.

Harmonic conversion can be achieved in 8-phase mixers by changing the effective phase of each baseband terminal depending on the harmonic to be upconverted. For the second harmonic, incrementing the baseband signals by 90° on each baseband port instead of the 45° used for the fundamental will result in operation identical to a 4-phase mixer with twice the LO frequency as shown in Fig. 6.2a. Since PA second harmonic terms will appear at $2F_{LO} + 2F_{IF}$, second harmonic cancellation also requires a baseband input at $2F_{IF}$. Similarly, third harmonic can be generated with 135° phase increments and injecting at $3F_{IF}$ on

each baseband port.

6.2.3 RX and TX Monitors

8-phase down-converting monitor circuits running on the TX LO are included at both ends of the distributed transmitter, providing direct access to the magnitude and phase of the TX signal at both ports, including 2nd and 3rd harmonics (Fig. 6.1). The ANT-end monitor has an attenuator to prevent saturation. On-chip monitors allow for quadrature, harmonic weight calculation from baseband signals without needing any external measurements or equipment.

6.2.4 Distributed Degeneration Network

While appropriate complex weighting of subtransmitters allows suppression of TX signals at the RX port, it does not provide rejection of noise and other perturbations in the individual transmit chains. In order to address this issue, [64] uses frequency-selective PA degeneration, which reduces PA noise in the RX band, but also greatly degrades output power when F_{TX} was placed too close to F_{RX}. Ideally sub-TX noise could be asymmetrically suppressed at the two ends of the transmission line similar to the TX signal. We achieve this by connecting the baseband terminals of the degeneration mixers to a shared bus. Complex weights are then applied to each degeneration mixer via a set of rotation multiplexers. Similar to suppression of the TX signal, appropriate selection of these complex weights suppresses noise at the receiver port without proportional TX gain suppression at the ANT port.

As shown in Fig. 6.3, complex weights were implemented by simple phase rotation. Switches steer the 8 baseband ports of each degeneration mixer to the shared bus in 45° steps. By steering the perturbations of any PA to the others with phase shifts that match those of the transmission line, the signal can be made to null at the receive port of the transmission line.

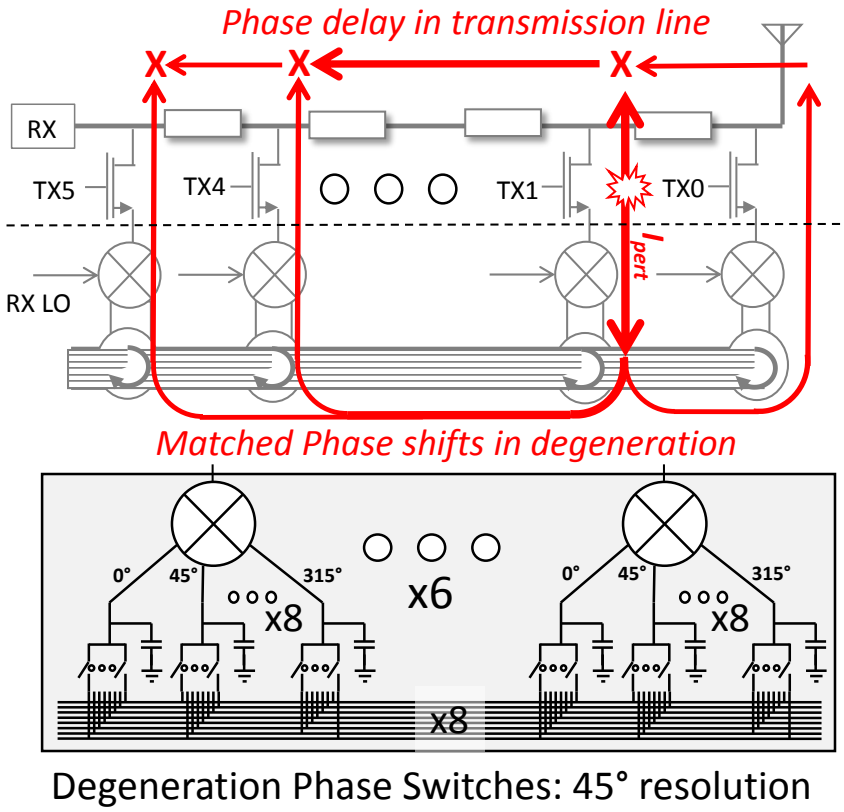


Figure 6.3: Distributed degeneration. The tap weights can be chosen accordingly to suppress TX noise. Phase rotations in distributed degeneration match delay in transmission line.

6.3 Measurement Results

6.3.1 Distributed Degeneration Measurements

To validate the proposed distributed degeneration approach, we compared different degeneration settings by looking at how signal injected from one PA travels differently to the antenna and receiver ports (Fig. 6.4). Compared to no degeneration, the individual degeneration technique from [64] recovers signal lost by the PA shunting and generates a notch at the RX frequency that reduces PA gain to both ports by >15dB compared to the out of band signal level.

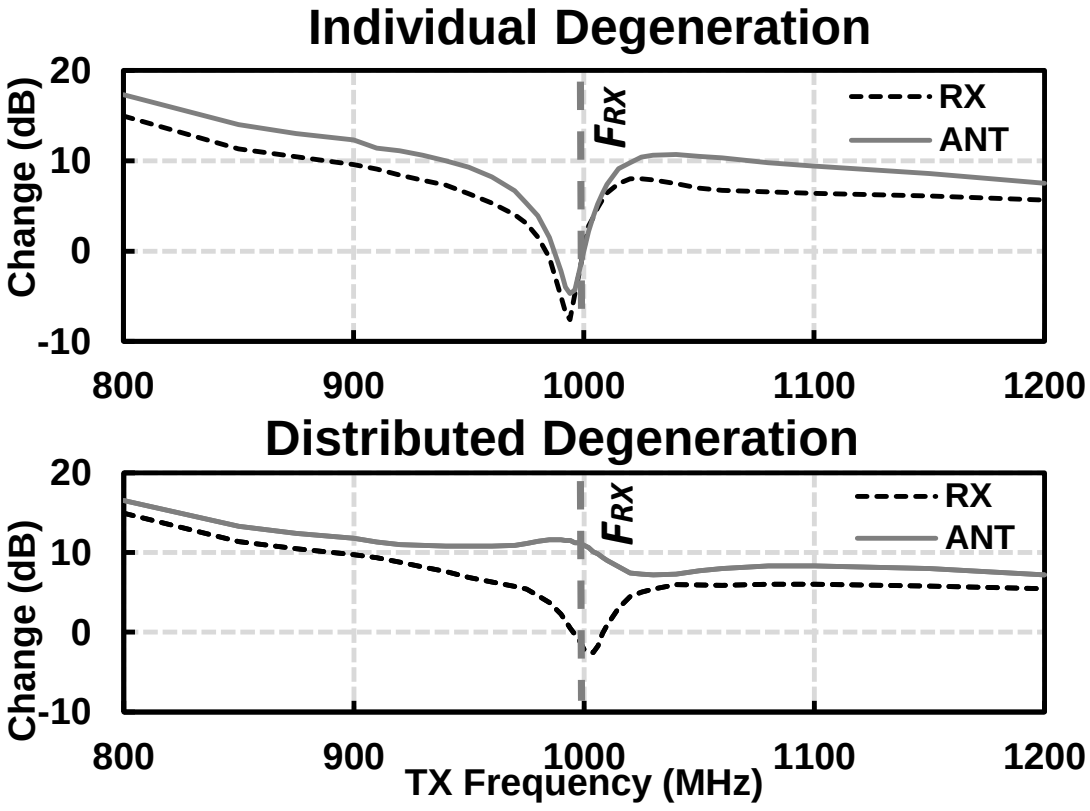


Figure 6.4: Impact of different degeneration modes on single PA gain to RX and ANT ports. Y-Axis is change in amplitude relative to gain with no degeneration.

Distributed degeneration has a similar impact on overall gain, and still produces a 12dB notch in PA gain to the RX port at the RX frequency, but now the PA gain to the antenna port actually slightly increases near the RX frequency.

6.3.2 Harmonic Predistortion Measurements

As shown in Fig. 6.5, for a fundamental output power of up to 18dBm, the second and third harmonic products can be suppressed to below -30dBm by predistortion, providing as much as 35dB improvement. Eventually the amount of baseband signal required to effectively null harmonics becomes greater than what the upconversion chain can supply, and so harmonic suppression degrades.

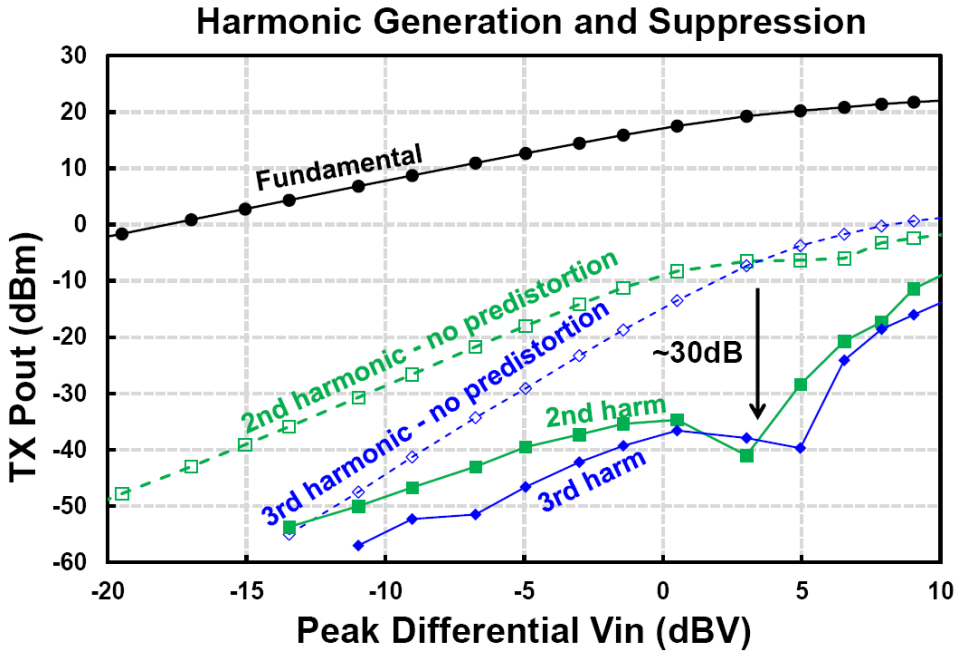


Figure 6.5: Suppression of second and third harmonics by the analog harmonic predistortion. The harmonics were suppressed for up to 30dB, pushing them below -30dBm levels.

Fig. 6.6 shows the duplexing performance of this system for an RX frequency of 1GHz. In TDD mode, no PA degeneration is engaged, allowing for the maximum TX gain of greater than 16dB from 800MHz to 1.2GHz. Without degeneration, NF is degraded by over 15dB due to TX noise at the RX frequency. The baseline, TX-off RX noise figure is high due unexpected loss at the transmission line interface caused by mis-modeling of the transmission line itself.

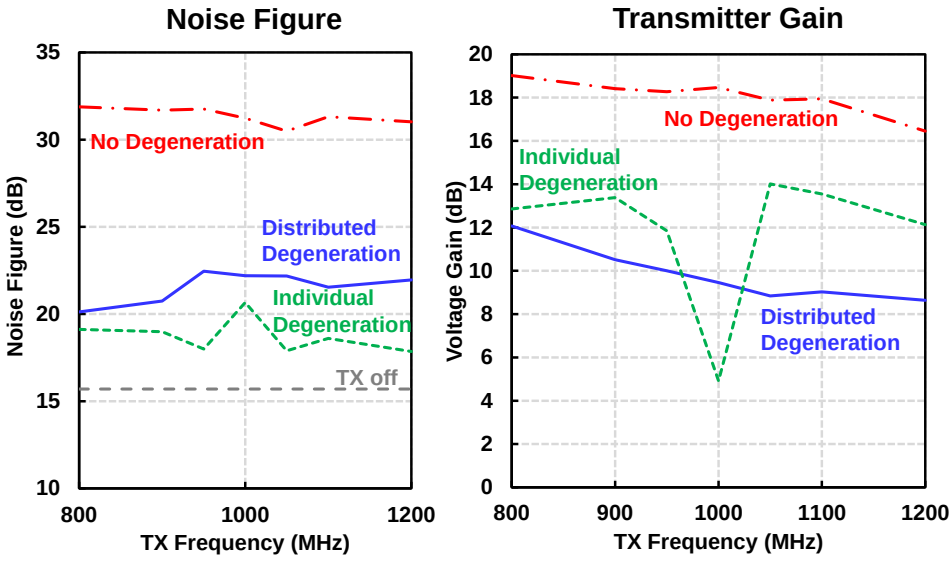


Figure 6.6: Duplexing performance across different RX-TX spacing. In the individual degeneration case, R_{sw} of mixers degenerates the PA out of band, while in the no degeneration case we short out the mixer switches to present a low degeneration impedance.

Engaging individual PA degeneration reduces TX gain, but improves RX NF degradation to only 5dB. For TX-RX spacing greater than 50MHz, TX gain stays above 11dB under individual degeneration, but falls as low as 5dB for sub 50MHz spacing. TX gain at spacing under 50MHz can be partially recovered using distributed degeneration. In FD mode, TX gain improves to 9.5dB, while NF degradation is comparable to the individual degeneration case at less than

7dB. In all cases a TX-RX isolation of >30dB is preserved.

Parameter	[7]	[70]	[68]	[64]	**This Work**
Max TX Power	8dBm	10dBm	25dBm	19dBm	23dBm
Technology	65nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS	28nm CMOS
Number of Antennas	1	2	1*	1	1
Operation Range	0.61-0.975GHz	0.15-3.5GHz	1.7-2.2GHz	0.3-1.6GHz	0.8-1.2GHz
TX/RX Isolation	40dB	27dB	55dB	25dB	30-456dB
Area	$0.94mm^2$	$2mm^2$	$3.5mm^2$	$12mm^2$	$23.1mm^2$
*Requires connecting a circulator connecting TX-RX					

Table 6.1: Performance Comparison to the State of the Art

6.4 Conclusion

We demonstrated a dual-chip, integrated, and software-defined front end capable of supporting TDD, FDD, and FD modes (Fig. 6.7) where FD mode is enabled through a novel degeneration network. This technique improves upon transmit gain previously lost by frequency selective degeneration.

The effect of harmonic terms on the RX has not been previously addressed in similar duplexers. Here, we presented a predistortion scheme that can be used to mitigate TX nonlinearity, preventing RX saturation due to PA harmonics.

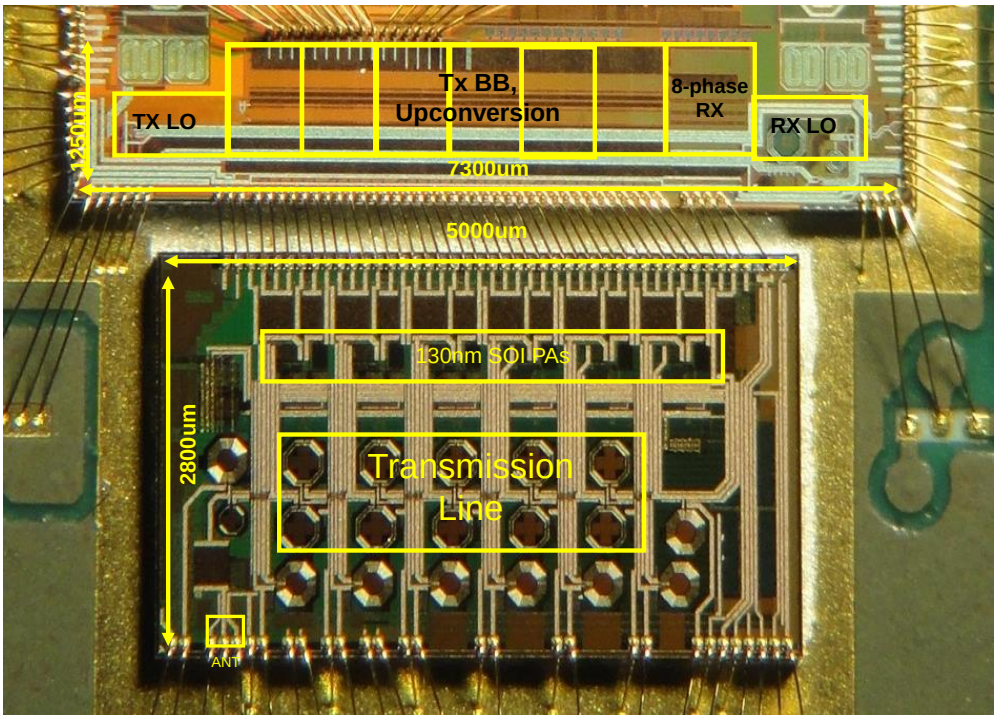


Figure 6.7: Dual chip die photo. The bottom chip contains the PAs and the transmission line.

CHAPTER 7

CONCLUSION

In this work, we have demonstrated two widely-tunable, software-defined duplexing radios capable of FDD and FD. These transceivers maintain >30 dB of isolation, while achieving an output power of >+23 dBm. These radios are tunable over multiple octaves and have two degeneration modes that ensure suppression of TX generated noise in the RX band. The distributed sub-transmitter structure enables robustness towards changing antenna impedances and nonlinearities. Furthermore, we introduced a circuit-level technique that allows physically accurate predictions of harmonic nonlinearity products in passive mixer circuits.

7.1 Thesis Contributions

This work outlines a potential solution to the frequency-crowding problem by presenting a duplexing transceiver that is viable over multiple octaves, enabling a way to take advantage of whitespace spectrum dynamically while maintaining high output power levels. Specifically, this work:

- Identifies the physically inaccurate harmonic distortion behavior in compact models of switching circuits as the result of second order discontinuity in I_{ds}.
- Proposes a circuit-level modeling technique that is easily accessible by the circuit designer to accurately simulate harmonic distortion products in switching circuits.

- Demonstrates the viability of this approach for a single transistor and an 8-phase passive mixer.
- Proposes a transmission-line-based distributed amplifier that leverages tunable phase and gain inputs to null the signal at the receiver port and constructively add at the antenna port.
- Leverages a passive mixer based frequency selective degeneration technique to boost output impedance of the sub-transmitters and degenerate gain in the TX band to alleviate noise contributions of TX in the RX band.
- Describes the system parameters of the duplexing transceiver and relates them to the figures of merit such as isolation and efficiency.
- Provides a detailed analysis of noise sources of the transceiver and explains their contribution mechanisms.
- Demonstrates a system fabricated in 65 nm that operates up to 19 dBm with $>$25 dB of isolation over two octaves of tunability. Adaptability of input phase and gain allows for a 1:3 VSWR change in antenna impedance without loss of isolation.
- Demonstrates results from a second generation transceiver fabricated in 28 nm that achieves 24 dBm of power and $>$30 dB of isolation with harmonic suppression and novel degeneration technique that allows the RX and TX to overlap each other in frequency.

7.2 Future Research Opportunities for Duplexing Transceivers

There are several improvements and future avenues to explore with regards to this work:

- Use of the duplexing transceivers to inform new network designs, especially in the PHY layer.
- Demonstration of a technique that widens the distributed duplexing cancellation bandwidth by injecting the fundamental signal and its derivative.
- A full system demonstration that utilizes the RF cancellation technique in addition to analog and digital domain cancellation to achieve >100 dB of self-interference cancellation.
- Further investigation of predictive modeling in the absence of experimental MOSFET data to approximate the slope of the second derivative. Better MOSFET capacitance modeling for the schematic-level.
- Integration of a switching PA as the sub-transmitter structure to enable better efficiency and creation of a system where the PA amplifier rails and bias points are dynamically adjusted.
- Creation of a full-duplex transceiver that shares a single LO for better noise performance.
- Creation and utilization of a closed-loop algorithm to automatically suppress harmonics due to nonlinearities of the PA.
- Use of the duplexing transceivers to demonstrate novel functionality such as relaying for interference alignment or LO synchronization.
- Creation an $N \times N$ transmission line structure with sub-transmitter tap points for MIMO applications.

- Integration of DACs into the TX baseband structure for a more easily controlled and robust design.

BIBLIOGRAPHY

[1] "Auction of advanced wireless services (aws-3) licenses closes winning bidders announced for auction 97." [Online]. Available: https://apps.fcc.gov/edocs_public/attachmatch/DA-15-131A1.pdf

[2] "Cisco visual networking index: Forecast and methodology, 2016-2021." [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/complete-white-paper-c11-481360.pdf

[3] FCC.gov, "United states frequency allocation chart," 2018, [Online; accessed April 27, 2018]. [Online]. Available: https://www.ntia.doc.gov/page/2011/united-states-frequency-allocation-chart

[4] ifixit.com, "United states frequency allocation chart," 2018, [Online; accessed April 27, 2018]. [Online]. Available: https://www.ifixit.com/Teardown/Samsung+Galaxy+S9+Teardown/104322

[5] S. Ramakrishnan, "Design of integrated full-duplex wireless transceivers," Ph.D. dissertation, University of California at Berkeley, 5 2017.

[6] J. Zhou, T. H. Chuang, T. Dinc, and H. Krishnaswamy, "Integrated wideband self-interference cancellation in the rf domain for fdd and full-duplex wireless," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3015–3031, Dec 2015.

[7] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, "Highly-linear integrated magnetic-free circulator-receiver for full-duplex wireless," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 316–317.

[8] D. Bharadia, E. McMilin, and S. Katti, "Full duplex radios," in *ACM SIGCOMM Computer Communication Review*, vol. 43, no. 4. ACM, 2013, pp. 375–386.

[9] J. I. Choi, M. Jain, K. Srinivasan, P. Levis, and S. Katti, "Achieving single channel, full duplex wireless communication," in *Proceedings of the Sixteenth Annual International Conference on Mobile Computing and Networking*, ser. MobiCom '10. New York, NY, USA: ACM, 2010, pp.

1–12. [Online]. Available: http://doi.acm.org/10.1145/1859995.1859997

[10] M. Jain, J. I. Choi, T. Kim, D. Bharadia, S. Seth, K. Srinivasan, P. Levis, S. Katti, and P. Sinha, "Practical, real-time, full duplex wireless," in *Proceedings of the 17th annual international conference on Mobile computing and networking*. ACM, 2011, pp. 301–312.

[11] H. Krishnaswamy, G. Zussman, J. Zhou, J. Maraevi, T. Dinc, N. Reiskarimian, and T. Chen, "Full-duplex in a hand-held device: From fundamental physics to complex integrated circuits, systems and networks: An overview of the columbia flexicon project," in *2016 50th Asilomar Conference on Signals, Systems and Computers*, Nov 2016, pp. 1563–1567.

[12] B. Debaillie, D. J. van den Broek, C. Lavn, B. van Liempd, E. A. M. Klumperink, C. Palacios, J. Craninckx, B. Nauta, and A. Prssinen, "Analog/rf solutions enabling compact full-duplex radios," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 9, pp. 1662–1673, Sept 2014.

[13] H. Krishnaswamy and G. Zussman, "1 chip 2x the bandwidth," *IEEE Spectrum*, vol. 53, no. 7, pp. 38–54, July 2016.

[14] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, "In-band full-duplex wireless: Challenges and opportunities," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 9, pp. 1637–1652, Sept 2014.

[15] J. Diakonikolas and G. Zussman, "On the rate regions of single-channel and multi-channel full-duplex links," *IEEE/ACM Transactions on Networking*, vol. 26, no. 1, pp. 47–60, Feb 2018.

[16] J. Marasevic, J. Zhou, H. Krishnaswamy, Y. Zhong, and G. Zussman, "Resource allocation and rate gains in practical full-duplex systems," *IEEE/ACM Trans. Netw.*, vol. 25, no. 1, pp. 292–305, 2017.

[17] A. Apsel, A. Molnar, D. Yang, H. Yüksel, T. Tappen, E. Enroth, M. Mohiuddin, and Z. Boynton, "Challenges and approaches to software defined duplexing radio," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 2779–2782.

[18] E. Ahmed and A. M. Eltawil, "On phase noise suppression in full-duplex systems," *IEEE Transactions on Wireless Communications*, vol. 14, no. 3, pp. 1237–1251, March 2015.

[19] J. Zhou and H. Krishnaswamy, "A system-level analysis of phase noise in full-duplex wireless transceivers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2018.

[20] S. Hong, J. Brand, J. I. Choi, M. Jain, J. Mehlman, S. Katti, and P. Levis, "Applications of self-interference cancellation in 5g and beyond," *IEEE Communications Magazine*, vol. 52, no. 2, pp. 114–121, February 2014.

[21] B. van Liempd, B. Hershberg, K. Raczkowski, S. Ariumi, U. Karthaus, K. F. Bink, and J. Craninckx, "2.2 a 70dbm iip3 single-ended electrical-balance duplexer in 0.18um soi cmos," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.

[22] X. Zhang, W. Cheng, and H. Zhang, "Full-duplex transmission in phy and mac layers for 5g mobile wireless networks," *IEEE Wireless Communications*, vol. 22, no. 5, pp. 112–121, October 2015.

[23] K. Tan, Y. He, H. Shen, J. Zhang, and Y. Zhang, "Spectrum virtualization layer," Tech. Rep., January 2011. [Online]. Available: `https://www.microsoft.com/en-us/research/publication/spectrum-virtualization-layer/`

[24] V. R. Cadambe and S. A. Jafar, "Interference alignment and spatial degrees of freedom for the k user interference channel," in *Communications, 2008. ICC'08. IEEE International Conference on*. IEEE, 2008, pp. 971–975.

[25] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable rf interface," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 12, pp. 2696–2708, 2010.

[26] M. C. M. Soer, E. A. M. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta, "A 0.2-to-2.0ghz 65nm cmos receiver without lna achieving 11dbm iip3 and 6.5 db nf," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2009, pp. 222–223,223a.

[27] H. Khatri, P. Gudem, and L. Larson, "Distortion in current commutating passive cmos downconversion mixers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 11, pp. 2671–2681, 2009.

[28] ——, "Simulation of intermodulation distortion in passive cmos fet mixers," in *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International*, June 2009, pp. 1593–1596.

[29] K. Joardar, K. Gullapalli, C. Mcandrew, M. Burnham, and A. Wild, "An improved mosfet model for circuit simulation," *Electron Devices, IEEE Transactions on*, vol. 45, no. 1, pp. 134–148, 1998.

[30] W. Wu, W. Yao, and G. Gildenblat, *PSP-SOI: A Surface-Potential-Based Compact Model of SOI MOSFETs*. Springer Netherlands, 2010.

[31] M. B. Dastjerdi and H. Krishnaswamy, "A simplified cmos fet model using surface potential equations for inter-modulation simulations of passive-mixer-like circuits," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 132–135.

[32] P. Bendix, P. Rakers, P. Wagh, L. Lemaitre, W. Grabinski, C. Mcandrew, X. Gu, and G. Gildenblat, "Rf distortion analysis with compact mosfet models," in *Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004*, 2004, pp. 9–12.

[33] X. Li, W. Wu, A. Jha, G. Gildenblat, R. van Langevelde, G. D. J. Smit, A. Scholten, D. B. M. Klaassen, C. Mcandrew, J. Watts, C. Olsen, G. Coram, S. Chaudhry, and J. Victory, "Benchmark tests for mosfet compact models with application to the psp model," *Electron Devices, IEEE Transactions on*, vol. 56, no. 2, pp. 243–251, 2009.

[34] N. Scheinberg and A. Pinkhasov, "A computer simulation model for simulating distortion in fet resistors," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 19, no. 9, pp. 981–989, 2000.

[35] C. C. McAndrew, "Validation of MOSFET model Source Drain Symmetry," *IEEE Transactions on Electron Devices*, vol. 53, pp. 2202–2206, Sep. 2006.

[36] H. Yüksel, D. Yang, and A. Molnar, "A circuit-level model for accurately modeling 3rd order nonlinearity in cmos passive mixers," in *Radio Frequency Integrated Circuits Symposium, 2014 IEEE*, June 2014, pp. 127–130.

[37] M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P. V. Wesemael, T. Sano, T. Yamamoto, D. Hauspie, J. V. Driessche, and J. Craninckx, "A 5 mm^2 40 nm lp cmos transceiver for a software-defined radio platform," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2794–2806, Dec 2010.

[38] J. Craninckx, M. Liu, D. Hauspie, V. Giannini, T. Kim, J. Lee, M. Libois, B. Debaillie, C. Soens, M. Ingels, A. Baschirotto, J. van Driessche, L. van der

Perre, and P. Vanbekbergen, "A fully reconfigurable software-defined radio transceiver in 0.13mm cmos," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2007, pp. 346–607.

[39] B. Analui, T. Mercer, S. Mandegaran, A. Goel, and H. Hashemi, "A 50 mhz-6 ghz, 2×2 mimo, reconfigurable architecture, software-defined radio in 130nm cmos," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, June 2014, pp. 329–332.

[40] C. Andrews and A. C. Molnar, "A passive-mixer-first receiver with baseband-controlled rf impedance matching, <6db nf, and >27dbm wideband iip3," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb 2010, pp. 46–47.

[41] C. Andrews, L. Diamente, D. Yang, B. Johnson, and A. Molnar, "A wideband receiver with resonant multi-phase lo and current reuse harmonic rejection baseband," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1188–1198, May 2013.

[42] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly integrated and tunable rf front ends for reconfigurable multiband transceivers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 9, pp. 2038–2050, Sept 2011.

[43] M. Mikhemar, H. Darabi, and A. A. Abidi, "A multiband rf antenna duplexer on cmos: Design and performance," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2067–2077, Sept 2013.

[44] D. Yang, H. Yüksel, C. Newman, C. Lee, Z. Boynton, N. Paya, M. Pedrone, A. Apsel, and A. Molnar, "A fully integrated software-defined fdd transceiver tunable from 0.3-to-1.6 ghz," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 334–337.

[45] D. J. van den Broek, E. A. M. Klumperink, and B. Nauta, "19.2 a self-interference-cancelling receiver for in-band full-duplex wireless with low distortion under cancellation of strong tx leakage," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.

[46] J. Zhou, T. H. Chuang, T. Dinc, and H. Krishnaswamy, "19.1 receiver with >20mhz bandwidth self-interference cancellation suitable for fdd, coexistence and full-duplex applications," in *2015 IEEE International Solid-*

State Circuits Conference - (ISSCC) Digest of Technical Papers, Feb 2015, pp. 1–3.

[47] D. Yang, H. Yüksel, and A. Molnar, "A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1189–1202, May 2015.

[48] V. Aparin, G. J. Ballantyne, C. J. Persico, and A. Cicalini, "An integrated lms adaptive filter of tx leakage for cdma receiver front ends," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1171–1182, May 2006.

[49] J. Zhou, A. Chakrabarti, P. R. Kinget, and H. Krishnaswamy, "Low-noise active cancellation of transmitter leakage and transmitter noise in broadband wireless receivers for fdd/co-existence," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3046–3062, Dec 2014.

[50] T. FCC, "Auction 73 700mhz band." [Online]. Available: `http://wireless.fcc.gov/auctions/default.htm?job=auction_factsheet&id=73`

[51] Ericsson, "Mobile broadband for all: optimizing radio technologies." [Online]. Available: `https://www.ericsson.com/res/docs/whitepapers/mobile-broadband-for-all.pdf`

[52] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Hybrid transformer-based tunable differential duplexer in a 90-nm cmos process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1316–1326, March 2013.

[53] M. Mikhemar, H. Darabi, and A. Abidi, "An on-chip wideband and low-loss duplexer for 3g/4g cmos radios," in *2010 Symposium on VLSI Circuits*, June 2010, pp. 129–130.

[54] B. van Liempd, B. Hershberg, B. Debaillie, P. Wambacq, and J. Craninckx, "An electrical-balance duplexer for in-band full-duplex with >-85dbm in-band distortion at +10dbm tx-power," in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, Sept 2015, pp. 176–179.

[55] J. Zhou, N. Reiskarimian, and H. Krishnaswamy, "9.8 receiver with integrated magnetic-free n-path-filter-based non-reciprocal circulator and baseband self-interference cancellation for full-duplex wireless," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 178–180.

[56] A. Goel, B. Analui, and H. Hashemi, "Tunable duplexer with passive feed-forward cancellation to improve the rx-tx isolation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 536–544, Feb 2015.

[57] B. Xiang, X. Wang, and A. B. Apsel, "A reconfigurable integrated dispersive delay line (ri-ddl) in 0.13-/spl mu/m cmos process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 7, pp. 2610–2619, July 2013.

[58] ——, "On-chip demonstration of real time spectrum analysis (rtsa) using integrated dispersive delay line (iddl)," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, June 2013, pp. 1–4.

[59] C. Andrews, C. Lee, and A. Molnar, "Effects of lo harmonics and overlap shunting on n-phase passive mixer based receivers," in *2012 Proceedings of the ESSCIRC (ESSCIRC)*, Sept 2012, pp. 117–120.

[60] D. Yang, C. Andrews, and A. Molnar, "Optimized design of n-phase passive mixer-first receivers in wideband operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 11, pp. 2759–2770, Nov 2015.

[61] L. Duipmans, R. E. Struiksma, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Analysis of the signal transfer and folding in n-path filters with a series inductance," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 263–272, Jan 2015.

[62] S. Jayasuriya, D. Yang, and A. Molnar, "A baseband technique for automated lo leakage suppression achieving <80dbm in wideband passive mixer-first receivers," in *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*, Sept 2014, pp. 1–4.

[63] D. Yang, H. Yüksel, and A. Molnar, "A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1189–1202, May 2015.

[64] H. Yüksel, D. Yang, Z. Boynton, C. Lee, T. Tapen, A. Molnar, and A. Apsel, "A wideband fully integrated software-defined transceiver for fdd and tdd operation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1274–1285, May 2017.

[65] H. Yüksel, D. Yang, Z. Boynton, E. Enroth, T. Tapen, A. Molnar, and A. Apsel, "Broadly tunable frequency division duplex transceiver: Theory and operation," in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec 2016, pp. 688–691.

[66] B. Xiang, X. Wang, and A. B. Apsel, "A reconfigurable integrated dispersive delay line in 0.13um cmos process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 7, pp. 2610–2619, July 2013.

[67] T. Tapen, Z. Boynton, H. Yüksel, A. Apsel, and A. Molnar, "The impact of lo phase noise in n-path filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. PP, no. 99, pp. 1–14, 2017.

[68] T. Zhang *et al.*, "18.1 a 1.7-to-2.2GHz full-duplex transceiver system with >50dB self-interference cancellation over 42MHz bandwidth," in *2017 IEEE ISSCC*, Feb. 2017, pp. 314–315.

[69] K. Fang and J. F. Buckwalter, "A tunable 5-7 GHz distributed active quasi-circulator with 18-dBm output power in CMOS SOI," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 11, pp. 998–1000, Nov. 2017.

[70] D. J. van den Broek *et al.*, "19.2 a self-interference-cancelling receiver for in-band full-duplex wireless with low distortion under cancellation of strong TX leakage," in *2015 IEEE ISSCC*, Feb. 2015, pp. 1–3.